Am486® Microprocessor PCI Customer Development Platform

User's Manual

Order #22408A

AMD

Am486® Microprocessor PCI Customer Development Platform User's Manual

IF YOU HAVE QUESTIONS, WE'RE HERE TO HELP YOU.

The AMD customer service network includes U.S. offices, international offices, and a customer training center. Technical assistance is available from the AMD worldwide staff of field application engineers and factory support staff to answer E86™ and Comm86™ microcontroller family hardware and software development questions.

Frequently accessed numbers are listed below. Additional contact information is listed on the back of this manual. AMD's WWW site lists the latest phone numbers.

Technical Support

Answers to technical questions are available online, through e-mail, and by telephone.

Go to AMD's home page at www.amd.com and follow the Service link for the latest AMD technical support phone numbers, software, and Frequently Asked Questions.

For technical support questions on all E86 and Comm86 products, send e-mail to **epd.support@amd.com** (in the US and Canada) or **euro.tech@amd.com** (in Europe and the UK).

You can also call the AMD Corporate Applications Hotline at:

(800) 222-9323	Toll-free for U.S. and Canada
44-(0) 1276-803-299	U.K. and Europe hotline

WWW Support

For specific information on E86 and Comm86 products, access the AMD home page at **www.amd.com** and follow the **Embedded Processors** link. These pages provide information on upcoming product releases, overviews of existing products, information on product support and tools, and a list of technical documentation. Support tools include online benchmarking tools and CodeKit™ software—tested source code example applications. Many of the technical documents are available online in PDF form.

Questions, requests, and input concerning AMD's WWW pages can be sent via e-mail to **webmaster@amd.com**.

Documentation and Literature Support

Data books, user's manuals, data sheets, application notes, and product CDs are free with a simple phone call. Internationally, contact your local AMD sales office for product literature.

To order literature, call:

(800) 222-9323	Toll-free for U.S. and Canada
(512) 602-5651	Direct dial worldwide
(512) 602-7639	Fax

Third-Party Support

AMD FusionE86^{SM} program partners provide an array of products designed to meet critical time-to-market needs. Products and solutions available include emulators, hardware and software debuggers, board-level products, and software development tools, among others. The WWW site and the *E86 Family Products Development Tools CD*, order #21058, describe these solutions. In addition, mature development tools and applications for the x86 platform are widely available in the general marketplace.

Contents

About the Customer Development Platform

Chapter 1

Quick Start

Chapter 2

Board Functional Description

Appendix A

Default Settings

Appendix B

Bill of Materials and Schematics

Index

List of Figures

List of Tables

About the Customer Development Platform

Congratulations on your decision to design with the Am486® microprocessor. The Am486 microprocessor PCI customer development platform (CDP) provides a reference design for embedded Am486 microprocessor-based systems using the Peripheral Component Interconnect (PCI) bus with an onboard 10- or 100-Mbit/s Ethernet connection.

The PCI CDP includes 9 Mbytes of Flash memory, PCI and ISA expansion connectors, and standard PC peripherals to allow customers to develop and benchmark network-ready firmware and applications for their embedded products. In addition, the platform's use of low cost, off-the-shelf components makes it a suitable example for use in training or as a reference for customer hardware designs.

The PCI CDP demonstrates that a fifth-generation x86 microprocessor is not required to include a PCI bus in customer designs.

Note: *Advanced Micro Devices does not assume any responsibility for the maintenance of this evaluation tool. Changes to the schematics will be made only if the board is required to go back through a CAD layout.*

Refer to the Am486 microprocessor documentation (listed on page xviii) for detailed information on the Am486 microprocessor.

Figure 0-1 on page xii provides an overview of the PCI CDP's features.

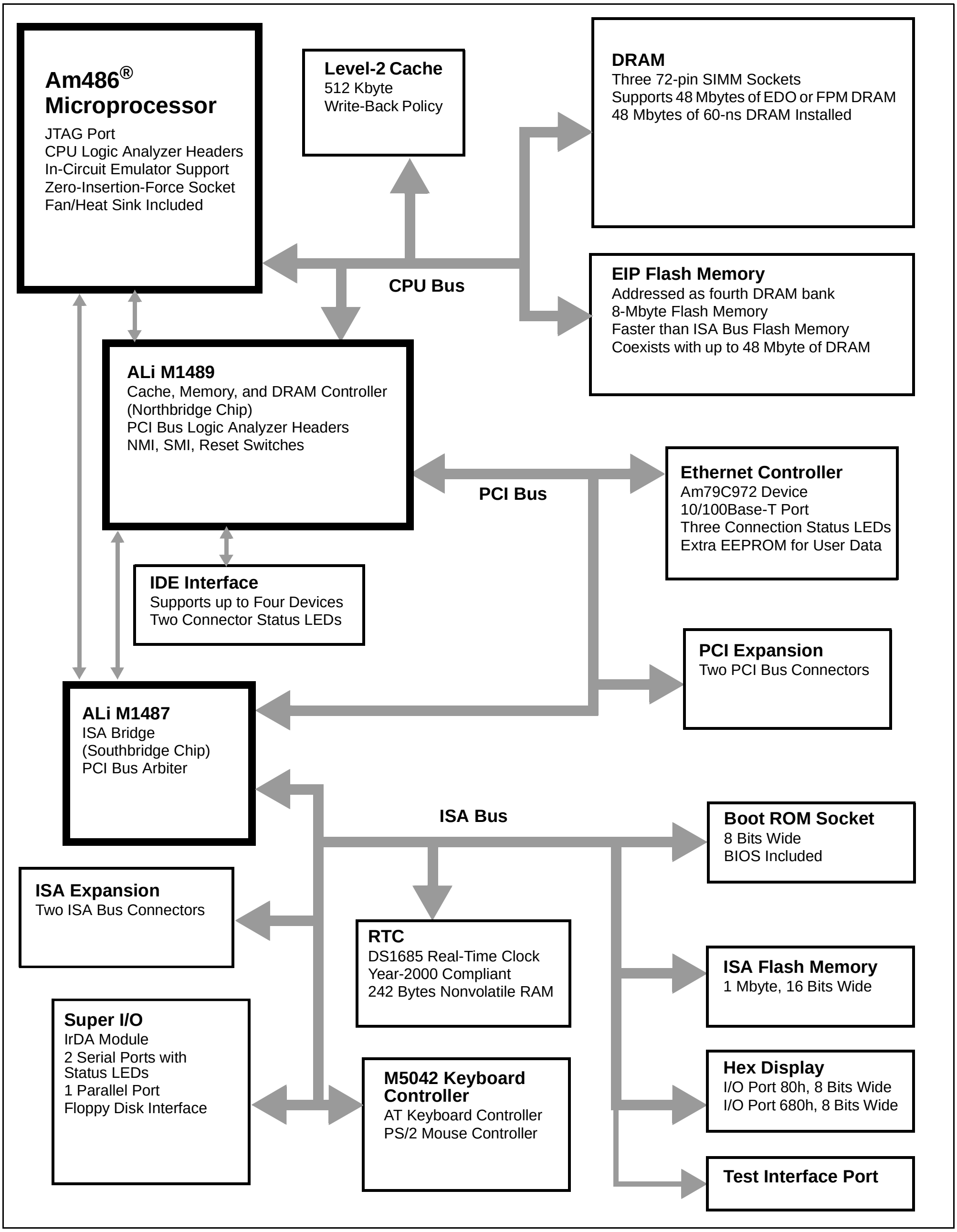


Figure 0-1. PCI CDP Overview

Evaluation Board Features

This section describes the following features of the PCI CDP:

Am486® Microprocessor

- AMD Am486 DX5 microprocessor is included. Supports Am486 DX2, DX4, and DX5 microprocessors (168-pin pin-grid array (PGA), 3.3 V or 3.45 V).
- Zero insertion force (ZIF) PGA microprocessor socket for emulator support.
- CPU voltage is jumper selectable.

Core Logic Chipset

- Acer Labs FINALi 486 PCI chipset
  - M1489 Cache, Memory, and PCI Controller
  - M1487 ISA Bridge Controller
  - M5402 Mouse/Keyboard Controller

DRAM Main Memory

- 48 Mbyte of 60-ns EDO DRAM installed.
- Supports one, two, or three banks of 32- or 36-bit-wide DRAM using industry standard 5-V 72-pin SIMMs. DRAM can be fast page mode (FPM) or extended data out (EDO).
- Supports 1-, 4-, or 16-Mbit technology DRAMs.
- Three SIMM sockets. One or two banks per socket. Three banks DRAM maximum.
- DRAM is accessible by CPU and PCI bus masters.
- L1/L2 cache snoop cycles are generated for PCI master memory accesses.
- Wait-state timing is configurable through chipset registers.

Boot ROM and Flash Memory

- Dip socket provided for one 8-bit-wide boot ROM, logically on the ISA bus.
- 1 Mbyte of 16-bit-wide Flash memory soldered to the board, logically on ISA bus.
- 8-Mbyte Flash memory for execute-in-place (EIP) applications, located on the memory bus in place of one DRAM bank. EIP Flash is implemented using an AMD 22V10 PAL® device for glue logic.

Onboard L2 Cache

- 512-Kbyte cache size, configured as 32-bit-wide memory.
- Write-back or write-through protocol configurable through chipset registers.
- One 32-Kbyte x8 SRAM for cache tag space, soldered to board.
- Four 128-Kbyte x8 SRAMs for cache data space, soldered to board.
- 2-1-1-1 (read) and 2-2-2-2 (write) burst timing with 15-ns data and 10-ns tag SRAMs.

PC and DOS Compatibility

- IDE interface in chipset.
- Standard chipset configuration registers, known to BIOS and DOS.
- Off-the-shelf PC chipset provides common I/O functions found in a PC:
  - Two 82C59 interrupt controllers (SMI, NMI, and INT support)
  - One 82C54 programmable interval timer
  - Two 82C37 DMA controllers (seven channels)
  - External boot ROM chip-select signal
  - PC-style real-time clock (RTC) (non-Y2K-compliant, disabled by default)
- DS1285 Y2K-compliant RTC chip. The DS1285 RTC can be disabled, and the non-Y2K RTC enabled, by removing one resistor and populating another.

PC-Style Super I/O

- DOS and PC-AT compatible I/O.
- Two 16550-compatible serial ports.
- One parallel port. Supports enhanced parallel port (EPP) and extended capabilities port (ECP) modes.
- Floppy disk interface.
- IrDA port with external transceiver (115 Kbyte/s).

Keyboard and Mouse Controller

- 8042-compatible controller chip (included in chipset).
- AT keyboard interface.
- PS/2 Mouse interface.

Onboard 10/100-Mbit/s Ethernet

- AMD PCnet™-Fast+ Ethernet Controller Chip, Am79C972.
- 32-bit PCI bus interface with bus mastering capability.
- Integrated 12-Kbyte buffer.
- External PHY transceiver for full duplex operation at 10 or 100 Mbit/s.
- IEEE802.3, PC97, PC98, and NetPC compliance.
- Preprogrammed 1-Kbyte serial EEPROM included for Ethernet configuration.
- Extra 4-Kbyte serial EEPROM included for user nonvolatile data.

Expansion Bus Support

- Two PCI 2.0 expansion connectors, desktop PC style.
- Two ISA 16-bit expansion connectors, desktop PC style.

Development Support

- In-circuit emulator (ICE) support with socketed microprocessor in PGA package.
- Logic analyzer headers for all CPU and PCI bus signals.
- Switches (push-button) for NMI, SMI, and RESET.
- LEDs for IDE, serial port, Ethernet activity, and Ethernet link speed.
- I/O port 80h and 680h hexadecimal displays.
- Am486 microprocessor JTAG support.
- Connector for AMD embedded systems Test Interface Port (TIP) board.

Form Factor

- Baby-AT motherboard form factor.
- Fits standard desktop-PC-style chassis.

BIOS and Software

The included diskette contains information about the included BIOS and any additional utility and demonstration software for the PCI CDP.

Customer Development Platform Documentation

The *Am486® Microprocessor PCI Customer Development Platform User's Manual* provides information on the design and function of the development platform. The software shipped with the board is described in the README files and online BIOS manual included with your kit.

The included online documentation is in text or Adobe Acrobat (PDF) format. The latest Acrobat Reader is available from Adobe's site on the World Wide Web (currently at **www.adobe.com**).

About This Manual

Chapter 1, "Quick Start" helps you quickly set up and start using the PCI CDP.

Chapter 2, "Board Functional Description" contains descriptions of the basic sections of the evaluation board: layout, microprocessor, core logic chipset, Ethernet controller, DRAM, boot ROM and Flash memory, PCI bus and ISA bus interfaces, super I/O, keyboard and mouse, drives, and interrupt switches.

Appendix A, "Default Settings" summarizes the jumper and configuration resistor positions on the PCI CDP when it is shipped.

Appendix B, "Bill of Materials and Schematics" shows the bill of materials for the evaluation board, and the actual CAD schematics used to build the board.

Suggested Reference Material

The following AMD documentation may be of interest to the PCI CDP user. For information on ordering literature, see page iii.

- *Enhanced Am486®DX Microprocessor Family Data Sheet*, order #20736
- *Am486®DX/DX2 Microprocessor Hardware Reference Manual*, order #17965
- *Am486® Microprocessor Software User's Manual*, order #18497
- *Am79C972 PCnet™-FAST+ Enhanced 10/100 Mbps PCI Ethernet Controller with OnNow Support Data Sheet*, order #21485
- *E86 Family Products Development Tools CD*, order #21058
- *Flash Memory Products Data Book*, order # 11796
- For current application notes and technical bulletins, see our World Wide Web page at **www.amd.com**.

The following non-AMD documents are also recommended:

- *Application Note 77: DS1585/87, DS1685/87, and DS17x85/87 Accessing Extended User RAM via Software*
  Dallas Semiconductor, **www.dalsemi.com**.
- *DS1685/DS1687 3 Volt/5 Volt Real Time Clock Data Sheet*
  Dallas Semiconductor, **www.dalsemi.com**.
- *FINALi 486 M1489/1487 PCI Chip Set Preliminary Data Sheet*
  Acer Laboratories Inc., see **www.acerlabs.com** for contact information. Related BIOS guidelines, errata, and application documents are also available.
- *M5113: Enhanced Super I/O Controller Data Sheet*
  Acer Laboratories Inc., see **www.acerlabs.com** for contact information.

Documentation Conventions

The Advanced Micro Devices *Am486® Microprocessor PCI Customer Development Platform User's Manual* uses the conventions shown in Table 0-1 (unless otherwise noted). These same conventions are used in all the E86 family support product manuals.

Table 0-1. Notational Conventions

Symbol	Usage
Boldface	Indicates that characters must be entered exactly as shown, except that the alphabetic case is only significant when indicated.
Italic	Indicates a descriptive term to be replaced with a user-specified term.
`Typewriter face`	Indicates computer text input or output in an example or listing.
[ ]	Encloses an optional argument. To include the information described within the brackets, type only the arguments, not the brackets themselves.
{ }	Encloses a required argument. To include the information described within the braces, type only the arguments, not the braces themselves.
..	Indicates an inclusive range.
...	Indicates that a term can be repeated.
|	Separates alternate choices in a list — only one of the choices can be entered.
:=	Indicates that the terms on either side of the sign are equivalent.

Chapter 1

Quick Start

This chapter provides information that helps you quickly set up and start using the Am486® microprocessor PCI customer development platform (CDP).

The PCI CDP is shipped with a BIOS that has been configured specifically for the chipset used on this platform. The BIOS contains the code that enables the PCI CDP to function as a standard AT-compatible PC, using AT-compatible displays, display adapters, and keyboards. Details on the BIOS can be found in the BIOS documentation shipped on diskette with your kit.

The PCI CDP can run AT-compatible operating system software. You can start the system with either a bootable diskette or an ATA (IDE) hard disk drive that already has the operating system installed.

Embedded BIOS software typically supports the configuration of onboard Flash memory as a resident flash disk (RFD) that can also be set up as a boot device. See the online BIOS manual included with your kit.

For information on how to:

- Set up the PCI CDP, see page 1-2.
- Boot the PCI CDP from a diskette, see page 1-6.
- Boot the PCI CDP from a hard disk drive, see page 1-7.
- Troubleshoot installation problems, see page 1-8.

Setting Up the PCI CDP

CAUTION: As with all computer equipment, the PCI CDP may be damaged by electrostatic discharge (ESD). Please take proper ESD precautions when handling any board.

Warning: Read before using this development platform

Before applying power, the following precautions should be taken to avoid damage or misuse of the board:

- Make sure power supply connectors (from a standard AT system power supply) are plugged onto the board correctly. The grounds (usually black wires) *must* meet at the center of the two power supply connectors on the board. See “Power Supply Connectors (N2 and P2)” on page 2-33.
- See Figure 2-3 on page 2-5 for connector positions.
- Check the diskette that was shipped with your kit for README or errata documentation. Read all the information carefully before continuing.

For current application notes and technical bulletins, see the AMD World Wide Web page at **www.amd.com** and follow the link to Embedded Systems.

Installation Requirements

You need to provide the following items (in addition to the PCI CDP from the kit).

Required for all setups:

- A VGA-compatible monitor
- A PCI- or ISA-bus video card that supports VGA
- A cable to connect the monitor to the video card
- An AT-compatible keyboard
- A PS/2-style mouse (if needed for your operating system)
- A standard AT-style power supply

To boot from a floppy diskette:

- An AT-compatible 3.5-inch or 5.25-inch diskette drive
- A bootable DOS diskette
- A standard 34-wire AT diskette drive cable

To boot from a hard disk drive:

- An ATA-compatible hard disk drive
- AT-compatible operating system (preinstalled on the hard disk drive)
- A standard 40-pin ATA HDD cable

If you install both a floppy diskette drive and a hard disk drive, you can boot from either device. Only one boot disk image (floppy or hard disk) is required. For example, you can boot from the floppy and then install the operating system on a blank hard disk drive.

CAUTION: Use the configuration described here when you first start the PCI CDP. Before using other features, read the appropriate sections in Chapter 2, “Board Functional Description.”

Board Installation

Note: *See Figure 2-2 on page 2-4 for a block diagram of the board. See Figure 2-3 on page 2-5 for a layout diagram of the board, including connector locations referenced in this section.*

DANGER: Make sure the power supply and the VGA monitor are *not* plugged into an electrical outlet during the following steps.

1. Remove the board from the shipping carton. Visually inspect the board to verify that it was not damaged during shipment. The board contains several jumpers. The following steps assume all jumpers are in the factory default configuration (settings are listed in Appendix A, “Default Settings”).

2. If you are installing a diskette drive, perform the following steps:

   a. Inspect the 34-wire, diskette-drive cable that you are providing. The red wire along one edge of the ribbon cable indicates wire 1. Most cables have a connector for the board at one end and two or more connectors along the length. There may be two different drive connectors at each location to accommodate different drive types.

   b. Connect one end of the diskette-drive cable to the 34-pin connector (connector J6 at location E20) on the PCI CDP (with wire 1 oriented towards the middle of the board). If there is a twist in one span of the cable, connect the opposite end to the board.

   c. Connect another connector on the diskette-drive cable to the diskette drive, just as you would for a standard PC installation. If there is a twist in the cable, the position you use determines whether the drive responds as A or B (typically drive A connects to the end of the cable, beyond the twist). The connector’s orientation should be indicated in the drive documentation, or marked near the connector on the drive. Usually wire 1 is oriented towards the drive’s power cable connector.

   d. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the diskette drive just as you would for a standard PC installation.

3. If you are installing a hard disk drive, perform the following steps:

   a. Inspect the 40-wire IDE cable that you are providing. The red wire along one edge of the ribbon cable indicates wire 1.

   b. Connect one end of the 40-wire IDE cable to the hard drive just as you would for a standard PC installation. The connector's orientation should be indicated in the drive documentation, or marked near the connector on the drive. Usually wire 1 is oriented towards the drive's power cable connector.

   c. Connect the other end of the 40-wire IDE cable to the first 40-pin connector (connector J5 at location L4) on the PCI CDP (with wire 1 oriented towards the edge of the board, near the power supply connector).

   d. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the hard drive just as you would for a standard PC installation.

4. Make sure the CPU heat sink is securely attached to the microprocessor and connect the heat sink fan power wires to a spare disk drive power connector. *Fan power supply connectors are not all the same. Check the voltage printed on the fan and connect its wires to the correct voltage pins on the appropriate power supply connector.*

5. Insert a PCI- or ISA-bus VGA-compatible video card into an appropriate slot on the PCI CDP. The PCI slots are labeled SLT1 and SLT2. The ISA slots are labeled SL1 and SL2.

6. Connect the monitor cable from the monitor to the D-connector on the video card just as you would for a standard PC.

7. Connect the AT keyboard to the keyboard connector (connector J1 at location O1).

8. Connect the PS/2 mouse (if used) to the mouse connector (connector J11 at location M1).

9. Connect the connectors (usually marked P8 and P9) from the standard PC power supply into the board's power connectors J2 (at location Q2) and J3 (at location N2). P8 connects to J2 (the six pins closest to the corner of the board); P9 connects to the other six pins. *Make sure the black ground wires from P8 and P9 meet in the middle of the board's J2 and J3 connectors.*

CAUTION: Failure to verify the power supply connections can result in total destruction of the PCI CDP.

Starting from Diskette

Use the following steps to start the PCI CDP from a bootable diskette:

1. Make sure you have installed the PCI CDP correctly as described in “Setting Up the PCI CDP” on page 1-2.

CAUTION: Failure to verify the power supply connections can result in total destruction of the PCI CDP.

2. Plug the VGA monitor into an electrical outlet and turn it on.
3. Insert a bootable DOS diskette (not included) in the disk drive.
4. Apply power to the PCI CDP by connecting the PC power supply to an electrical outlet. If the power supply is equipped with a switch, turn it on.

   The power supply fan should start running, and the port 80h LEDs should start to display power-on self-test (POST) status codes. Then the speaker should beep and the monitor should start displaying startup information.

   Make sure the CPU heat sink fan is running. *Do not operate the microprocessor without a functioning heat sink fan.*

5. The first time you start the system, the BIOS might display a message reporting a CMOS error or some other BIOS configuration problem. Follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system’s date, time, startup drive, and other options.

   For more information on the included BIOS, see the online BIOS manual included with your kit.

6. Save and exit the setup utility.
7. The system should now boot from the DOS diskette just like a standard PC. If you encounter any problems, see “Installation Troubleshooting” on page 1-8.

Starting from an IDE Hard Drive

Use the following steps to start up the PCI CDP from an IDE hard drive on which you have preinstalled an operating system (while it was connected to another PC):

1. Make sure you have installed the PCI CDP correctly as described in “Setting Up the PCI CDP” on page 1-2.

   CAUTION: Failure to verify the power supply connections can result in total destruction of the PCI CDP.

2. Plug the VGA monitor into an electrical outlet and turn it on.
3. If a diskette drive is installed, make sure it is empty.
4. Apply power to the PCI CDP by connecting the PC power supply to an electrical outlet. If the power supply is equipped with a switch, turn it on.

   The power supply fan and hard disk should start running, and the port 80h LEDs should start to display power-on self-test (POST) status codes. Then the speaker should beep and the monitor should start displaying startup information.

   Make sure the CPU heat sink fan is running. *Do not operate the microprocessor without a functioning heat sink fan.*

5. The first time you start the system, the BIOS might display a message reporting a CMOS error or some other BIOS configuration problem. Follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system’s date, time, startup drive, and other options.
6. In the BIOS setup utility, use the automatic configuration option to set up Drive C. Select either physical addressing or logical block addressing (LBA) as appropriate for your hard disk drive.

   For more information on the included BIOS, see the online BIOS manual included with your kit.

7. Save and exit the setup utility.
8. The system should now boot using the operating system on the hard disk. If you encounter any problems, see “Installation Troubleshooting” on page 1-8.

Installation Troubleshooting

Table 1-1. Installation Troubleshooting

Problem	**Solution**
The Port 80h LED readout is blank after I turn on the power supply.	Check power supply connectors J2 and J3.
The Port 80h LED readout is stuck at 00. I see nothing on the VGA monitor and do not hear any beeps from the speaker. I do not hear the head synchronization on the diskette drive (if attached).	Ensure processor reset by pressing the Reset button, SW1 at location N5. Check that the BIOS ROM and the microprocessor are correctly installed, and that jumpers JP32 and JP33 are both off.
The Port 80h LED readout displayed some power-on-self-test (POST) numbers, but then stopped at one number before the system finished starting.	Make sure all cables are connected properly, all adapters are seated firmly in their slots, and the CMOS battery is correctly installed. See the online BIOS documentation included with your kit for a list of POST numbers and meanings.
I hear a beep on the speaker but see nothing on the VGA monitor.	Check that the monitor is plugged in and turned on. Check that the monitor is correctly connected to the video card. Check that the video card is correctly seated in the appropriate slot. Check that the video card supports VGA.
I see the startup information on the monitor but the memory test stops at an incorrect memory size. (1 Mbyte equals 1024 Kbyte.)	Make sure the SIMMs that came with the kit are securely installed in the SIMM sockets.
I see the startup information on the monitor but it says there's a battery problem or CMOS checksum error and the system doesn't finish booting.	Follow the BIOS instructions to run the Setup utility to configure the CMOS RAM and save settings.

Table 1-1. Installation Troubleshooting (Continued)

Problem	Solution
I configured the CMOS RAM and saved my settings, but settings are lost the next time I turn on the PCI CDP.	Make sure a fresh 3.0-V 20-mm coin cell is installed correctly (“+” side facing up) in the BT1 battery holder at location E12.
I don’t hear any sound from the diskette drive and the system does not boot from a diskette.	Check that the 34-wire cable to the diskette drive is properly connected at both the drive end and the board end (board connector J6 at location E20). The red wire should be oriented towards pin 1 on both the drive and the board. Check that the CMOS setup indicates that drive A is the correct size and capacity for your diskette drive.
I hear the diskette being accessed but get an error message “Non System disk” or “Drive A not found.”	Check that the diskette in the drive is bootable, just as you would on a standard PC. Make sure the diskette drive is connected properly to the last connector on the cable. In the BIOS setup utility, make sure the BIOS is configured to boot from diskette, and that the diskette size and density is configured properly.
I get a “Missing Keyboard” error message on the monitor during boot-up.	Check that an AT-style keyboard is properly connected.
The BIOS debugging monitor prompt is displayed.	Make sure the NMI switch is not pressed. Check that the DRAM and any PCI or ISA-bus devices are installed correctly and known to be functional.

Table 1-1. Installation Troubleshooting (Continued)

Problem	Solution
I have installed a hard disk with a preinstalled operating system, but the PCI CDP won't access the hard disk.	Check that the 40-wire IDE cable is properly connected at both the drive end and the board end (board connector J5 at location L4). Check that the CMOS setup is configured correctly for your drive. Make sure the board will start from a bootable diskette in drive A. Then try to do a directory listing of drive C. If the directory listing of C works, the drive is functioning and there is a problem with the drive's boot block or system image. (Note that some operating systems will display an error if you list an empty directory. If this happens, try copying a file to the drive; then do a directory listing again. If this fails, check the drive for boot block viruses.) Make sure the drive functions properly on a different system.
There is a problem you cannot resolve.	Check that the board is set to its default settings (see Appendix A, "Default Settings"). Contact the AMD Technical Support Hotline (see page iii).

Chapter 2

Board Functional Description

The Am486® microprocessor PCI customer development platform (CDP) provides a test and development platform for Am486 microprocessor-based designs. Read the following sections to learn more about the board:

See the appendices for information about default board settings, bill of materials, and schematics.

Feature and Layout Diagrams

The following figures summarize the features and layout of the PCI CDP.

- Figure 2-1 on page 2-3 provides an overview of the platform's features.
- Figure 2-2 on page 2-4 is the block diagram for the platform.
- Figure 2-3 on page 2-5 shows the platform layout and component locations.

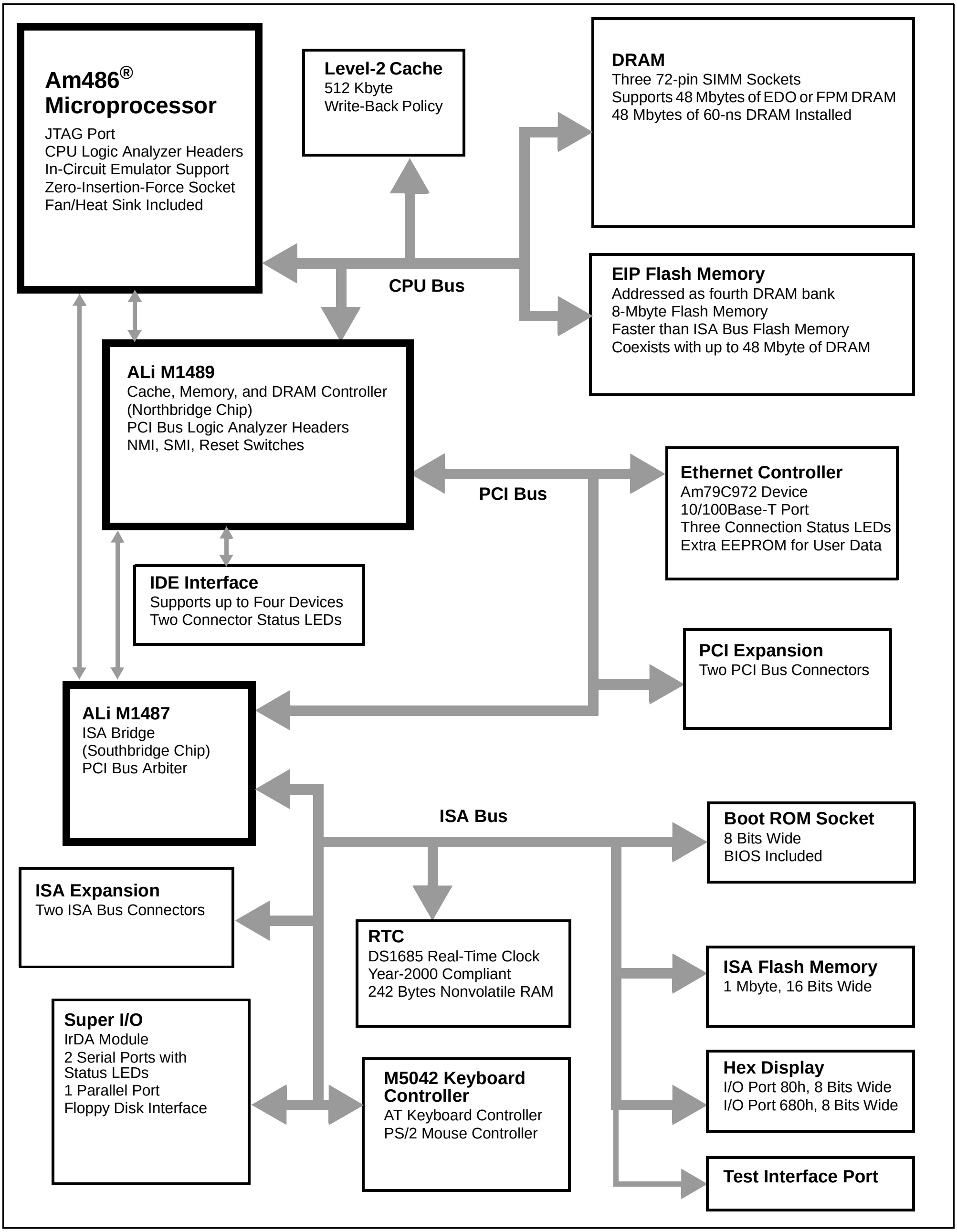


Figure 2-1. PCI CDP Overview (Same as Figure 0-1)

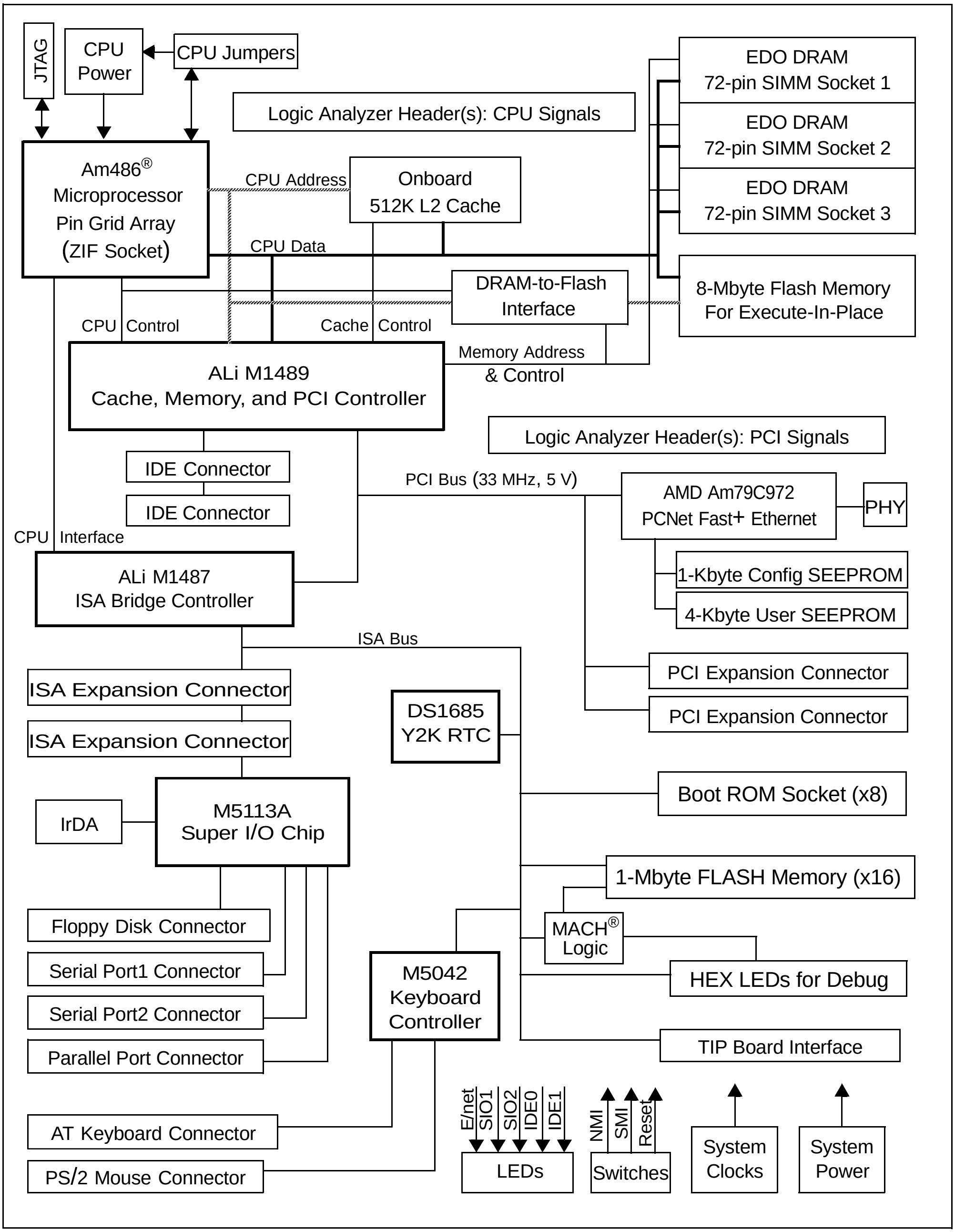


Figure 2-2. PCI CDP Block Diagram

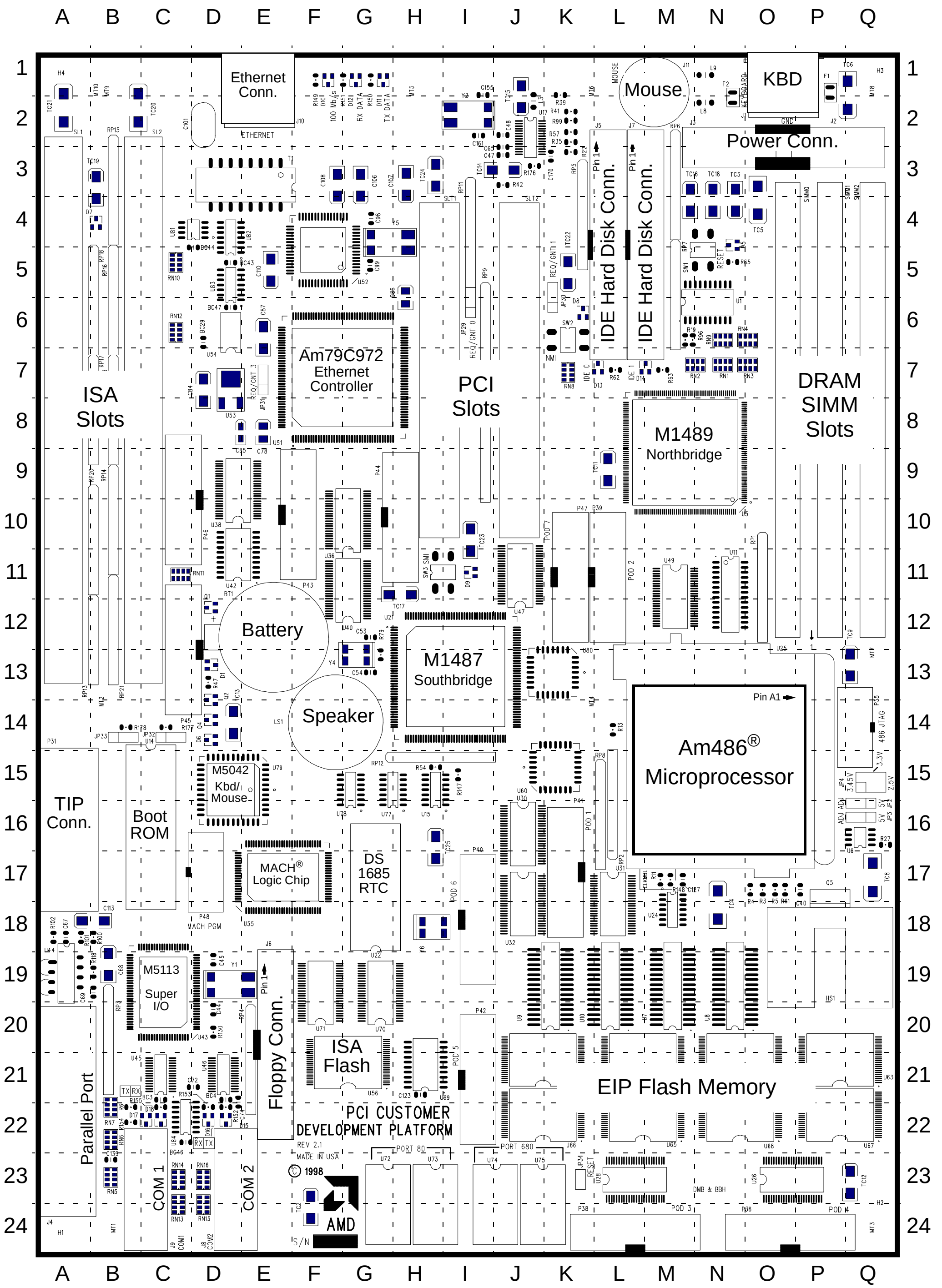


Figure 2-3. PCI CDP Layout

Jumper Functions

Table 2-1 describes the configuration jumpers on the PCI CDP.

Table 2-1. Board Jumper Summary

Part	Signal	Description	Location in Figure 2-3 on Page 2-5	See App. B Schematics on:	For More Info., See:
JP2	CPUV$_{CC}$3	Used with JP3 to select either 5-V CPU voltage or the adjustable voltage set by jumper JP4. *Both JP2 and JP3 must be positioned the same.*	Q15	Sheet 3	page 2-32
JP3	CPUV$_{CC}$3	Used with JP2 to select either 5-V CPU voltage or the adjustable voltage set by jumper JP4. *Both JP2 and JP3 must be positioned the same.*	Q16	Sheet 3	page 2-32
JP4	CPUV1, CPUV2, CPUV3	Selects the CPU voltage used when JP2 and JP3 are set to “ADJ.” The selectable voltages are 3.45 V, 3.3 V, and 2.5 V.	R15	Sheet 3	page 2-32
JP32	Boot ROM A17	Used to configure boot ROM address signal A17.	C14	Sheet 17	page 2-21
JP33	Boot ROM A18	Used to configure boot ROM address signal A18.	B14	Sheet 17	page 2-21

Board Restrictions

- Using a PCI chipset with the Am486 microprocessor is a fast and effective way to design a working system, but the system's features can be limited by the chipset's capabilities.
- The chipset used in the PCI CDP supports 5-V PCI 2.0 devices only. Three devices are supported: the onboard Ethernet controller and two PCI slots.
- Except for the adjustable CPU supply voltage and 3.3-V Ethernet controller, the PCI CDP uses 5-V power throughout. (The Am486 microprocessor provides 5-V-tolerant I/O.)
- The chipset does not directly support ROM or Flash memory devices except for the boot ROM. It is possible to implement Flash memory on the DRAM, PCI or ISA bus, but the chipset only allows booting from the boot ROM. ISA-bus Flash memory is limited to 1 Mbyte because of addressing considerations.
- The PCI CDP implements two banks of execute-in-place (EIP) Flash memory in place of one DRAM bank. Flash memory timing requirements limit the chipset's DRAM interface to its Fast (not Fastest) speed when the Flash memory is used. This is equivalent to using 70-ns fast-page-mode (FPM) DRAM.
- The chipset allows only three banks of DRAM to be attached without external buffers. Buffering the DRAM adds one wait state and reduces the available performance. "DRAM Main Memory (P7)" on page 2-20 describes additional DRAM device and configuration limits.
- The ISA peripherals provided by the M1487 chip are configured for standard PC-AT compatibility, so there is not much flexibility in assigning interrupts and DMA channels.
- The PCI CDP does not implement OnNow or Advanced Configuration and Power Interface (ACPI) power management.

Board Features

The remainder of this chapter describes the features of the PCI CDP. The number in parentheses following each heading indicates the part's location in Figure 2-3 on page 2-5. In addition, other locations referenced can be found in the figure.

Am486 Microprocessor (M14)

The PCI CDP includes an Am486 microprocessor in a 168-pin, pin-grid-array package (part U25). The microprocessor is zero-insertion-force (ZIF) socketed and a CPU fan heat sink is provided for cooling. For debugging and analysis, access is provided to the Am486 microprocessor's JTAG debugging port and to all of the microprocessor signals, and support is provided for Intel-compatible in-circuit emulators. See "Development Support" on page 2-15.

The Enhanced Am486DX Microprocessor Family boosts system performance by incorporating a 16-Kbyte cache to the existing flexible clock control and enhanced System Management mode (SMM) features of a 486 CPU. The Enhanced Am486DX Microprocessor Family has the following characteristics:

- Industry-standard write-back cache support
- Frequent instructions execute in one clock
- 105.6-million bytes/second burst bus at 33 MHz
- Flexible write-through and write-back address control
- Advanced 0.35-µ CMOS-process technology
- 3.3-V or 3.45-V core with 5-V tolerant I/O
- Dynamic data bus sizing for 8-, 16-, and 32-bit buses (the PCI CDP uses a 32-bit data bus)
- 32-bit address bus
- 32-bit registers
- Supports "soft reset" capability
- 16-Kbyte unified code and data cache
  - Four-way set-associative
  - Write-through or write-back policy (the PCI CDP uses write-back policy)
- Floating-point unit
- Paged, virtual memory management
- Stop clock control for reduced power consumption
- Industry-standard two-pin System Management Interrupt ($\overline{\text{SMI}}$) for power management independent of processor operating mode and operating system

- Static design with Auto Halt power-down support
- Wide range of chipsets supporting SMM available to allow product differentiation (the PCI CDP uses the Acer Laboratories Inc. FINALi 486 chipset)
- Support available through the AMD FusionE86 Program

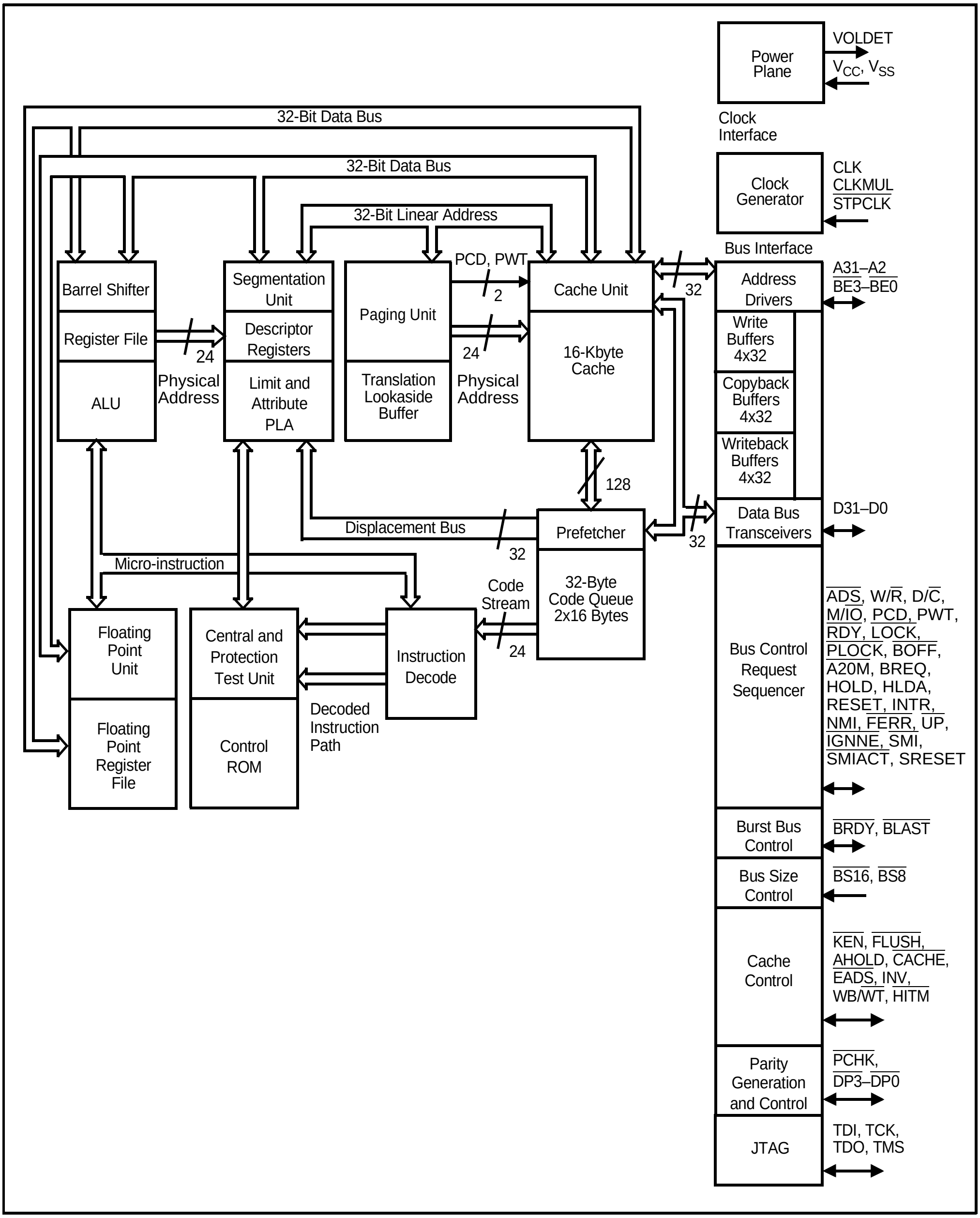


Figure 2-4. Am486 Microprocessor Block Diagram

Core Logic Chipset (M8, I13, D15)

The PCI CDP uses the Acer Laboratories Inc. FINALi 486 chipset. The chipset consists of two very-large-scale-integration (VLSI) devices that provide bus interface and peripheral functions used in the system, plus an M5042 keyboard and mouse controller. See “Keyboard (O1)” on page 2-31.

The M1489 Cache, Memory, and PCI Controller (often called a *northbridge* chip) interfaces the Am486 microprocessor to the memory and PCI bus. The M1489 (part U5 at location M8) performs the following functions:

- Controls DRAM accesses and refresh cycles. See “DRAM Main Memory (P7)” on page 2-20
- Provides a 33-MHz, PCI 2.0-compliant interface with 5-V signalling. See “PCI Bus (I7)” on page 2-19
- Maintains Level-1 and Level-2 cache coherency for PCI-master-initiated memory cycles. See “Level-2 Cache Memory (K19–N19 and N11)” on page 2-20
- Provides an IDE controller for a hard disk drive. See “IDE Hard Drive (L4 and M4)” on page 2-31

The PCI CDP routes three PCI address signals via series resistors to the $\overline{\text{IDSEL}}$ pins on the two PCI slots and the onboard Ethernet controller. The chipset asserts one of these signals to configure each device according to the device number written to the chipset’s configuration address register. Table 2-2 relates each device to its device number and signal routing.

Table 2-2. PCI Configuration Addressing

PCI Device	Device Number	PCI Address Signal	PCI ID Select Signal	See App. B schematics on:
Slot SLT1	Device 3	PAD19	PCIID1	Sheet 11
Slot SLT2	Device 4	PAD20	PCIID2	Sheet 11
Ethernet Controller	Device 5	PAD21	PCIID3	Sheet 11, Sheet 13

All PCI bus signals are routed to logic analyzer headers. See "Development Support" on page 2-15.

The M1487 ISA Bridge Controller (often called a *southbridge* chip) interfaces the ISA bus to the PCI bus and provides standard, PC-compatible peripherals devices common to desktop computers. The M1487 (Part U21 at location I13) provides the following peripheral functions:

- Two 82C59 interrupt controllers
- One 82C54 programmable interval timer
- Two 82C37 DMA controllers
- A real-time clock (RTC) (optional on the CDP, see "Real-Time Clock (G17)" on page 2-27)
- External boot ROM decoding

The M1487's integrated peripherals are configured for standard PC-AT compatibility, so there is not much flexibility in assigning interrupts and DMA channels.

The M1487 also contains the PCI bus arbiter, which allows three additional masters. The PCI CDP board uses one master request/grant interface for the onboard Am79C972 Ethernet controller. The other two master interfaces are routed to the PCI expansion slots.

The M1489 and M1487 communicate with each other across their proprietary LinkBus. The LinkBus has no separate pins, but instead uses the CPU address pins A2 to A17. The LinkBus handles the RTC, keyboard controller, and boot ROM transactions as well; this is why CPU address pins are routed to these devices in the schematics. The chipset asserts the Am486 microprocessor's AHOLD input to three-state its address pins when the LinkBus is in use.

Onboard Ethernet Controller (F7)

The PCI CDP includes an onboard, full-duplex 10/100BaseT Ethernet port based on the AMD Am79C972 PCnet™-*FAST+* Ethernet Controller (part U51). A separate voltage regulator provides 3.3-V power for the Ethernet controller. The Ethernet port is part J10 at location E1 on the board. Three LEDs near the port indicate transmit and receive activity and link speed. The link LED lights if 100 Mbit/s operation is established.

The Ethernet controller's interrupt output (INTA) is routed to the chipset's PCI INT2 signal. The initialization code dynamically assigns INT2 to an interrupt request (IRQ) in the chipset's PCI INTx routing table mapping registers. See the chipset documentation for details on the mapping registers.

The Am79C972 PCnet-*FAST+* device is a highly integrated 10/100 Mbps PCI Ethernet controller. It includes an IEEE 802.3-compliant Ethernet Media Access Controller (MAC) with Auto-Negotiation of 10 or 100 Mbps and half- or full-duplex operation, and a Media Independent Interface (MII) for connection to any standard IEEE 802.3 compliant 10/100 Mbps physical layer (PHY) device.

The Am79C972 contains a high performance 32-bit PCI bus master interface, as well as large, flexible internal memory buffers, to provide high-speed data throughput and low CPU and system bus utilization. For PCI configuration, the Ethernet controller is accessed as device number 5.

The Am79C972 can be configured by the PCI configuration space mechanism or it can download its configuration from a 1-Kbyte serial EEPROM (part U54 at location D6). The PCI CDP uses the serial EEPROM interface to configure the Am79C972 device. The EEPROM is preprogrammed with an Ethernet configuration suitable for the PCI CDP.

In addition to the Ethernet configuration EEPROM, a 4-Kbyte serial EEPROM is provided for user nonvolatile data. See "4-Kbyte Serial EEPROM (C4)" on page 2-14.

For customer designs, the PCnet-*FAST+* controller is offered with AMD's extensive suite of industry-proven PCnet software drivers, remote boot ROM firmware (not supported by the PCI CDP), and a complete set of supporting utilities and design tools. Follow the **Networking** link at **www.amd.com** for information about networking software, support, and tools.

The PCnet-*FAST+* device supports the industry's Net PC specification. The PCnet-*FAST+* device also complies with Microsoft's PC97 and PC98 requirements by fully supporting the OnNow and ACPI power management initiatives; however, the PCI CDP does not implement OnNow or ACPI. A customer design could support these technologies by using an ATX-style power supply and motherboard design.

4-Kbyte Serial EEPROM (C4)

An extra NM93C66M8 4-Kbyte serial EEPROM (part U81) is connected to the Am79C972 Ethernet controller's serial EEPROM interface. This provides additional EEPROM space for storing user nonvolatile data.

The M1487 device's CLKCTL signal (controlled via chipset register 40h) is used to multiplex the Ethernet controller's EEPROM chip select between the 1-Kbyte EEPROM and the 4-Kbyte EEPROM. When CLKCTL is asserted (the default), the Ethernet controller's 1-Kbyte configuration EEPROM (part U54) is accessed normally. When CLKCTL is deasserted, the Ethernet controller's EEPROM interface registers can be used to access the 4-Kbyte EEPROM to store or retrieve user data. See Sheet 13 of the schematics in Appendix B.

Software for using the 4-Kbyte EEPROM is provided with the PCI CDP. See the readme file on the diskette that came with your kit for information about available utilities.

Development Support

The PCI CDP includes the following facilities for development support:

- JTAG port
- CPU-bus and PCI-bus logic analyzer headers
- Port 80 and Port 680 hexadecimal displays
- TIP board interface

These features are described in the following paragraphs.

JTAG Ports (Q14 and D17)

The Am486 microprocessor provides an IEEE Standard 1149.1-1990 (JTAG) compliant test access port and boundary-scan architecture. The JTAG port provides a scan interface for testing the microprocessor in a production environment. The microprocessor's JTAG port is available on connector J35 at location Q14.

Do not attempt use the second JTAG port (part P48 at location D17). This port is used at AMD to program the Vantis™ MACH® programmable logic device. Reprogramming of the MACH device can cause improper system operation. The MACH device controls the ISA Flash memory space and the Port 80h and 680h hexadecimal displays. See "ISA Flash Memory (F20)" on page 2-23 and "Hexadecimal Display (H23, J23)" on page 2-17.

Logic Analyzer Headers

The CPU interface signals are buffered and routed to headers for a logic analyzer. The signals on the CPU bus logic analyzer headers are arranged to be compatible with the disassembler for the HP 16500 Logic Analyzer, but any analyzer can be used. Table 2-3 lists the available headers, their locations in Figure 2-3, and the Appendix B schematics sheet on which they appear. Sheet 4 of the schematics includes usage notes.

Table 2-3. Analyzer Headers

Part	Description	Location in Figure 2-3 on Page 2-5	See App. B Schematics on:
P36	POD 4, Microprocessor data (GD) signals	P24	Sheet 4
P38	POD 3, Microprocessor data (GD) signals	M24	Sheet 4
P39	POD 2, Microprocessor control signals, plus LA qualifier (see note on schematics Sheet 4)	L11	Sheet 5
P40	POD 6, Microprocessor address (GA) signals	I17	Sheet 5
P41	POD 1, Microprocessor control signals	K16	Sheet 5
P42	POD 5, Microprocessor address (GA) signals, including logic-derived GA0 and GA1 signals	I20	Sheet 5
P43	PCI Address and Data (PAD) signals	F11	Sheet 12
P44	PCI Address and Data (PAD) signals	H9	Sheet 12
P45	PCI control signals	C12–D13	Sheet 12
P46	PCI control signals	C9–D10	Sheet 12
P47	POD 7, Miscellaneous microprocessor control signals	K10	Sheet 4

In addition to the logic analyzer headers, separate three-pin headers are provided for each PCI device's bus request and bus grant signals. These headers are listed in Table 2-4:

Table 2-4. PCI Bus Master Test Points

Part	Signal	Location in Figure 2-3 on Page 2-5	See App. B Schematics on:
JP29	PREQJ0 PGNTJ0 GND	I6	Sheet 12
JP30	PREQJ1 PGNTJ1 GND	K5	Sheet 12
JP31	PREQJ2 PGNTJ2 GND	E7	Sheet 12

In-Circuit Emulator Compatibility (M14, Q15–Q16)

The PCI CDP can be used with an in-circuit emulator that mates to the pin-grid-array (PGA) zero-insertion-force (ZIF) socket in place of the Am486 microprocessor. To support emulators that use an Intel microprocessor, the necessary CPU power-supply jumpers are provided so the board will work with Intel 486 DX2 and DX4 chips. See "CPU Voltage Adjustment (Q15–Q16)" on page 2-32.

When connecting an in-circuit emulator, risers might be required to allow proper placement relative to the microprocessor socket and the ISA slots.

Hexadecimal Display (H23, J23)

The PCI CDP includes 2-digit hexadecimal displays for port 80h and port 680h debugging messages. To change the display value, perform an 8-bit write to I/O port 80h or 680h, respectively. The value written is latched by the display and cannot be read back by software.

Test Interface Port (TIP) (A16)

The PCI CDP includes a connector for the AMD Test Interface Port (TIP) board. The TIP board is used for testing and debugging AMD embedded product customer development platforms. It connects through a ribbon cable to the TIP connector on the platform.

The TIP board provides a collection of peripherals, such as LEDs, hexadecimal displays, an LCD display, two serial ports, a parallel port, an Ethernet controller, and Flash memory, that can be convenient in system development.

The PCI CDP's TIP connector resides on the ISA bus and can use the ISA interrupt request (IRQ) signals if a TIP board is connected. Individual TIP connector IRQ signals are listed in Table 2-5. See the TIP board documentation for I/O addressing information.

Table 2-5. TIP Interrupt Usage

TIP Function	Interrupt
TIP Ethernet	IRQ15
TIP parallel port	IRQ12
TIP serial port 1	IRQ11
TIP test function	IRQ14
TIP serial port 2	IRQ10

NOTE: The TIP board's IRQ usage can conflict with the PCI CDP's onboard PC peripherals. Some TIP or CDP peripherals may not operate correctly when the TIP board is in use.

PCI Bus (I7)

The PCI CDP has two desktop-PC-style PCI expansion connectors (parts SLT1 and SLT2) to allow the installation of a wide array of off-the-shelf 5-V PCI devices. These include standard devices such as video, sound, SCSI, or PCMCIA adapters, or diagnostic devices such as PCI bus analyzers, extender cards, and other diagnostic hardware. The slots do not support 3.3-V PCI peripherals. The PCI bus is implemented via the chipset's M1489 northbridge chip except for bus arbitration, which is handled by the M1487.

For PCI bus configuration, connector SLT1 is addressed as Device 3 and SLT2 is addressed as Device 4. See Table 2-2, "PCI Configuration Addressing," on page 2-11.

The PCI bus connector's interrupt signals are routed as shown in Table 2-6. (The Ethernet interrupt signal is also shown for reference.) The initialization code dynamically assigns PCI interrupts to an interrupt request (IRQ) in the chipset's PCI INTx routing table mapping registers. See the chipset documentation for details on the mapping registers.

Table 2-6. PCI Bus Interrupt Routing

PCI Bus Interrupt	PCI Slot 1 Signal	PCI Slot 2 Signal	Ethernet Signal
INT0	INTA	INTD	—
INT1	INTB	INTA	—
INT2	INTC	INTB	INTA
INT3	INTD	INTC	—

Level-2 Cache Memory (K19–N19 and N11)

The PCI CDP includes an onboard 512-Kbyte, single-bank, direct-mapped, unified Level-2 cache. This is the largest single-bank cache allowed by the chipset. The cache tag and data static RAM (SRAM) devices are soldered onto the PCI CDP board. A 10-ns tag SRAM device and 15-ns data SRAM devices are used to achieve 2-1-1-1 timing on reads and 2-2-2-2 on writes.

The tag SRAM is a single 32-K by 8-bit device, part U11, and the data SRAMs are 128-K by 8-bit devices, parts U7, U8, U9, and U10.

Chipset registers allow the level-2 cache to be disabled or enabled. The level-2 cache can be configured for either write-back or write-through operation.

NOTE: The benefit of level-2 cache varies, depending on the software being used.

DRAM Main Memory (P7)

The PCI CDP comes with three standard, 5-V, 72-pin single inline memory module (SIMM) sockets, populated with three 16-Mbyte, 60-ns, extended data out (EDO) SIMMs.

The included SIMMs provide the largest and fastest DRAM configuration allowed in this design. For customer designs, the SIMM configurations supported depend upon the chipset and the initialization or BIOS code used to configure the chipset's registers. See the chipset documentation for information about detecting and configuring DRAM. The BIOS provided will automatically detect the amount of DRAM installed.

The chipset used in this design supports 2-, 4-, 8-, 16-, or 32-Mbyte SIMMS using 4- or 16-Mbit technology DRAM chips. Either fast page mode (FPM) or EDO SIMMs can be used, and the sockets can be filled with a combination of FPM or EDO SIMMs. All installed SIMMs must be run at the same speed, however.

The chipset allows either 1, 2, or 3 DRAM banks. Single- and double-bank SIMMs can be combined as shown in Table 2-7 on page 2-21.

Table 2-7. SIMM Socket Population Chart

SIMM 0	SIMM 1	SIMM 2
Single Bank SIMM	Single Bank SIMM	Single Bank SIMM
Double Bank SIMM	Single Bank SIMM	—

NOTE: 32- or 36-bit-wide memory can be used. However, 36-bit EDO SIMMs are accessed as only 32 bits wide because the FINALi chipset does not support EDO SIMMs' 32-bit data plus 4-bit error correction code (ECC) format. Only traditional byte-wide parity is supported.

Boot ROM (C16)

The PCI CDP provides a 0.5-inch wide 32-pin DIP socket (part U14) for an initialization or BIOS ROM device. The boot ROM is implemented on the M1487 chip's LinkBus.

The boot ROM socket is populated with a BIOS that allows the PCI CDP to boot and run DOS, Windows, or a real-time operating system (RTOS) immediately.

The platform must always boot from the boot ROM because of chipset limitations. The chipset does not allow booting from another source such as DRAM-bus, ISA-bus, or PCI-bus memory.

The boot ROM address space size defaults to 128 Kbytes, using ROM device address bits A0–A16, but the board design provides jumpers JP32 and JP33 (at locations C14 and B14) for configuring the ROM device's A17 and A18 address signals. The jumpers allow these address bits to be left High, tied Low, or connected to their corresponding ISA bus signal. This provides flexibility in addressing various sized Flash memory or ROM devices. See Figure 2-5 on page 2-22

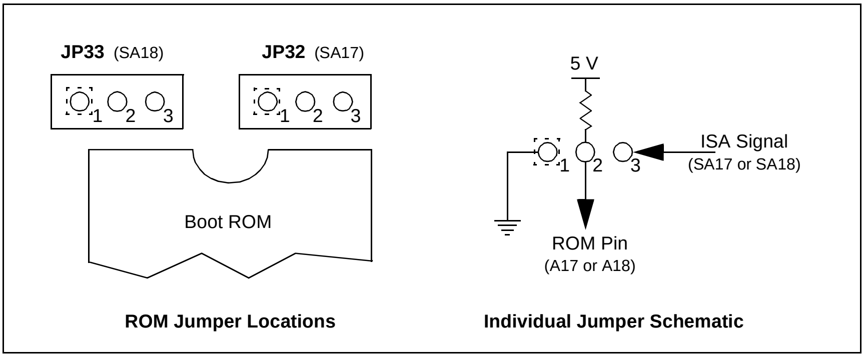


Figure 2-5. JP32 and JP33 Jumper Configuration (B14–C14)

By default, jumpers JP32 and JP33 are not connected, so ROM device pins A17 and A18 are tied High to address the 128-Kbyte BIOS range, E0000h–FFFFFh. If these jumpers are changed to select ISA addressing for addresses C0000h–DFFFFh, software must enable ROM addressing for this space via chipset register index 12h, bits 2–1, and index 44h, bits 7–6.

For software compatibility, the boot ROM image appears from E0000h to FFFFFh in the Am486 microprocessor's lower 1-Mbyte address space. (This assumes that a 128-Kbyte boot ROM is used.) At reset, however, the microprocessor is in a special state that causes it to fetch its first instruction from FFFFFFF0h, at the top of its extended memory range. To provide the first instruction, the boot ROM is aliased to begin at FFFE0000h. One of the first instructions is typically a far jump, which ends the special state and causes the microprocessor to continue execution in the lower 1-Mbyte space.

Because boot ROM accesses are relatively slow, subsequent initialization code typically copies the boot ROM contents into DRAM space and configures the chipset's Shadow Region Register to direct all boot ROM accesses to this shadow image of the boot ROM.

ISA Flash Memory (F20)

The PCI CDP includes 1 Mbyte of 16-bit wide AMD Flash memory soldered onto the board and located logically on the ISA Bus. A Vantis MACH programmable logic device is used to control the interface between the ISA bus and the Flash device. This provides an example of how a small amount of ISA Flash memory might be implemented in customer designs.

The ISA Flash memory employs one Am29F800 top-sector boot block Flash memory chip (part U58). This device occupies ISA memory space from address F00000h to FFFFFFh. See Figure 2-6 on page 2-24. Software should access this space in 16-bit words on even addresses.

Software can enable this ISA memory space by setting bit 3 of the chipset’s ROM Function Register, index 12h. This disables DRAM access in the 1-Mbyte range from F00000h to FFFFFFh, allowing access to the ISA memory space instead. If bit 3 of index 12h is clear, access to the ISA Flash memory space is allowed only if 15 Mbytes or less of DRAM is installed.

The Flash device is configured in word mode, so only 16-bit access is allowed. The ISA address signals are routed so that ISA address bit A1 is routed to bit A0 on the Flash device, so it can only be addressed on even word boundaries. When generating Flash command sequences, multiply the Flash address by two to generate the correct ISA address. For example, writing address F00AAAh asserts 555h (AAAh ÷ 2) on the Flash device’s address pins.

The Am29F800 can be programmed using the JDEC single-power-supply Flash standard command set. See the Am29F800 documentation for details. Software for using Flash memory is provided with the PCI CDP. See the readme file on the diskette that came with your kit for information about available utilities.

ISA space is limited to 16 Mbytes, and because the chipset provides limited support for mapping ISA memory windows over DRAM, only 1 Mbyte of Flash memory is provided. However, in a customer design with a small amount of DRAM, a larger ISA Flash memory space can be situated between the top of DRAM and the 16 Mbyte ISA address limit. Note that access to memory on the ISA bus is relatively slow when compared to DRAM or PCI bus transactions. See “EIP Flash Memory (L21)” on page 2-25 for another approach.

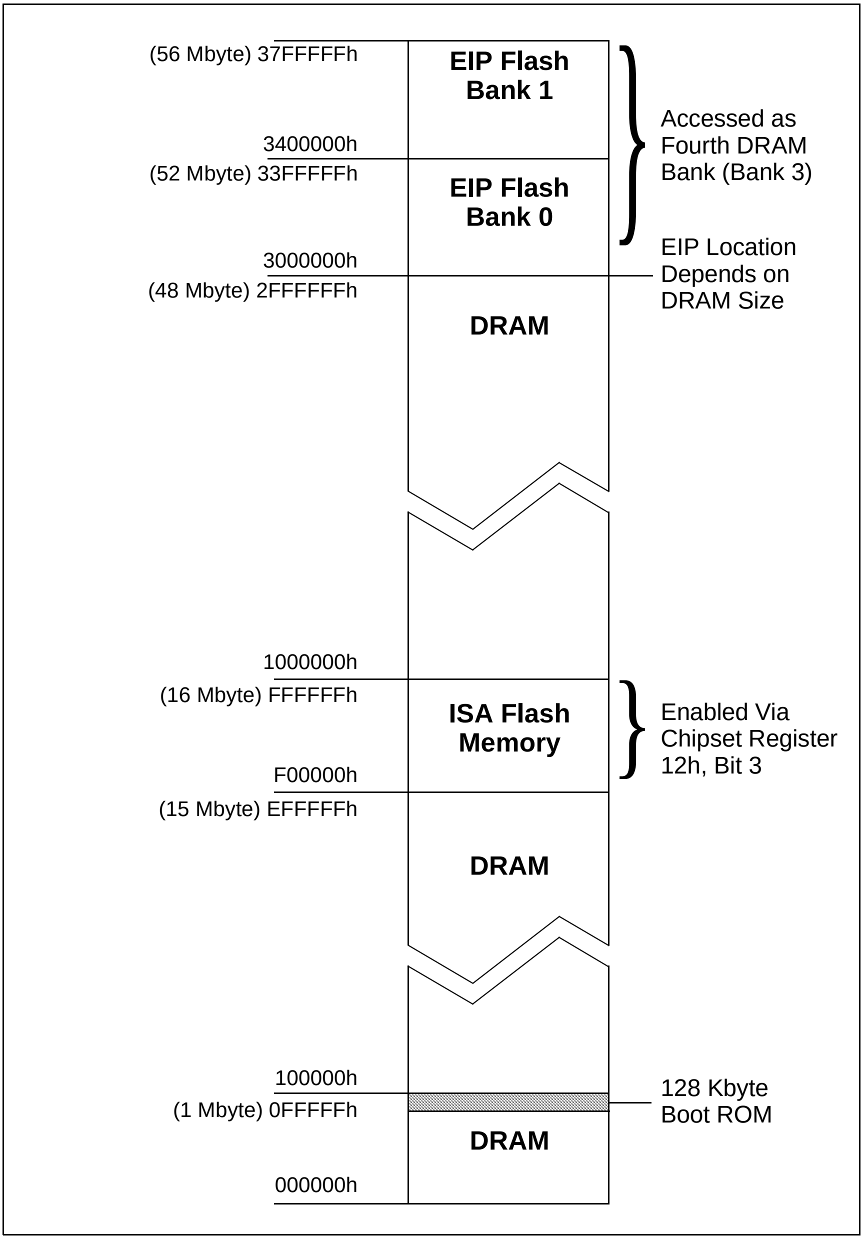


Figure 2-6. Typical Memory Map With ISA and EIP Flash Memory

EIP Flash Memory (L21)

The PCI CDP includes 8 Mbytes of Flash memory for execute-in-place (EIP) applications. The EIP Flash memory is implemented in the fourth bank (bank 3) of the DRAM controller’s address space. This memory consists of eight 29F800B top-sector boot block Flash memory devices (parts U61, U62, U63, U64, U65, U66, U67, and U68), soldered to the board and organized as two 32-bit wide Flash memory banks.

The EIP Flash memory is controlled by an AMD 22V10 PAL® device programmed to act as a simple DRAM-to-Flash interface that makes the Flash memory appear to the M1489 DRAM controller as a single bank of 32-bit-wide EDO DRAM.

The provided BIOS enables the EIP Flash memory and configures the other DRAM banks accordingly. To enable the EIP Flash memory, the BIOS programs the chipset’s DRAM Configuration Register 2 (index 11h, bits 4–7) so the fourth DRAM bank is accessed as 2-Mbyte by 8 (11 row, 10 column) DRAM chips. The DRAM-to-Flash interface uses CPU address bit A22 for Flash memory bank switching (A22 is routed to DRAM address bit 8 in the selected configuration). Because of timing requirements, it is also necessary to program the chipset’s DRAM Configuration and Timing Control registers (index 1Ah and 1Bh) to disable hidden refresh, disable $\overline{\text{RAS}}$-only refresh, select Fast access mode (not Fastest), and select $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh. This affects all four DRAM banks.

The EIP Flash memory can be accessed only by the CPU (no PCI bus-master access to the EIP Flash is allowed), and all accesses are 32 bits wide. During normal operation, the EIP Flash memory can be read like other DRAM memory, but data cannot be written directly. Instead, the Am29F800 devices are programmed using the JDEC single-power-supply Flash standard command set. See the Am29F800 documentation for details. Software for using Flash memory is provided with the PCI CDP. See the readme file on the diskette that came with your kit for information about available utilities.

Software that writes to the EIP Flash memory must make sure that accesses to the Flash memory are not cached. This can be done by disabling Level-1 and Level-2 memory caching, or by appropriate programming of the page tables if paging is enabled in the microprocessor.

Software that writes to the EIP Flash memory must also avoid any back-to-back write cycles (including back-to-back non-burst cycles) to the EIP Flash memory space. For reliable writes, always read or write a different DRAM bank (0, 1 or 2) before and after writes to the EIP space. For example, read location 00000h, write a value to Flash memory, and then read location 00000h again. (Simply running the Flash programming software in the normal DRAM space *does not* ensure reliable Flash programming, even though caching is disabled.)

Reading the EIP Flash memory does not entail any of the timing restrictions that apply to writes. The microprocessor can read EIP Flash memory with any combination of single-beat or burst read cycles.

The EIP Flash memory itself is organized in two banks. The base address of each EIP bank depends on how much DRAM is installed in DRAM banks 0–2. The board is shipped with 48 Mbytes installed, so by default the EIP first bank base address is 3000000h (48 Mbytes + 1 byte), and the EIP second bank base address is 3400000. See Figure 2-6 on page 2-24. Software can query the chipset's DRAM Configuration Registers (index 10h and 11h) to determine the size of banks 0–2. See the chipset documentation for a description of these registers.

Each Flash device is configured in byte mode, with four devices in each EIP bank. The CPU address signals are routed so that CPU address bit A2 is routed to bit A0 on the Flash devices, so the EIP space can only be addressed on even 4-byte (32-bit double-word) boundaries. When writing to the devices' control registers, multiply the byte-mode register offset by four to generate the correct CPU address. For example, if the bank base address is 3000000h, writing address 3002AA8h asserts AAAh (2AA8h ÷ 4) on each Flash device's address pins.

Real-Time Clock (G17)

The real-time clock (RTC) function in the chipset's 1487 chip is initially disabled on the PCI CDP. Instead, a separate DS1685 year-2000 (Y2K)-compliant RTC is enabled.

The DS1685 provides the features of widely-used, non-Y2K-compliant RTCs such as the DS1287. In addition, the DS1685 provides a byte for storing century information, plus other registers and features not found in older RTC chips.

Because of its extra features, the DS1685 RTC is not completely compatible with the DS1287. The provided BIOS operates correctly with the DS1685 RTC, but the extra RTC features can cause unexpected behavior if a customer-supplied BIOS is used in PC-AT compatible systems. One example is that the DS1685 provides some interrupt sources that are not present in the DS1287 RTC. Customer-written initialization software can take the following steps to disable the extended RTC interrupts:

1. Set the DV0 bit in CMOS register A to enable access to the extended register bank in the DS1685.
2. Write a value of 60h to CMOS address 4Bh to disable the extended interrupt addresses.
3. Clear the Dv0 bit in CMOS register a to disable access to the extended register bank (so that legacy software behaves as expected).
4. Read CMOS register C to clear any pending interrupts that were triggered while the extended interrupts were enabled.

For DS1685 RTC programming details, see the *DS1685/DS1687 3 Volt/5 Volt Real Time Clock Data Sheet*, and *Application Note 77: DS1585/87, DS1685/87, and DS17x85/87 Accessing Extended User RAM via Software*, available from Dallas Semiconductor, **www.dalsemi.com**.

If desired, the M1487's internal RTC can be enabled instead of the DS1685 by removing resistor part R58 from the back side of the board, beneath location I14. (See Sheet 16 of the schematics in Appendix B.)

ISA Bus Interface (A7)

The PCI CDP is populated with two standard ISA bus connectors (parts SL1 and SL2) for developers who need to use ISA devices in their development systems. The ISA bus interface is provided by the chipset's M1497 southbridge.

ISA devices that use the F00000h to FFFFFFh address space cannot be used on the PCI CDP, because this area is used by the ISA Flash memory bank. See "ISA Flash Memory (F20)" on page 2-23.

ISA devices that use the C0000h to DFFFFh address space cannot be used if this space is enabled for boot ROM addressing. See "Boot ROM (C16)" on page 2-21. Boot ROM addressing in this range might also cause conflicts with devices using the D0000h to DFFFF address space.

Super I/O (C19)

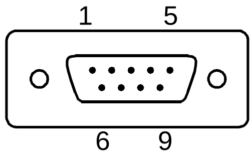
The PCI CDP uses an M5113 Super I/O chip to provide standard PC input/output functions. The Super I/O chip provides:

- Two 16450/16550-compatible serial ports
- IrDA 1.0 infrared interface
- AT-compatible parallel port
- 82077-compatible floppy disk interface

The BIOS supplied with the platform configures these peripherals to operate as they would on a standard PC. See the Acer Laboratories Inc. M5113 data sheet for detailed configuration information.

Serial Ports (E23 and C23)

The platform's Super I/O device includes two 16550-compatible serial ports. These are routed to two 9-pin D-shell connectors, J8 and J9. See Figure 2-7 and Table 2-8. Light-emitting diodes (LEDs) are provided near each serial port to indicate transmit and receive activity.



Notes:

See Figure 2-3 on page 2-5 for connector locations.

Figure 2-7. Serial Port Connector Pins (J8, J9)

Table 2-8. Serial Port Pin/Signal Table

Pin	Signal
1	$\overline{\text{DCD}}$
2	RXD
3	TXD
4	$\overline{\text{DTR}}$
5	GND
6	$\overline{\text{DSR}}$
7	$\overline{\text{RTS}}$
8	$\overline{\text{CTS}}$
9	$\overline{\text{RIN}}$

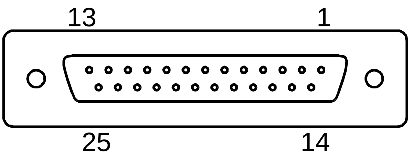
IrDA Interface (A19)

The Super I/O device is configured to support infrared data transfers via an IrDA LED module, part U44. The serial data transmission rates include all of the UART bit rates (up to 115 Kbps).

The IrDA LED module is connected to dedicated pins on the M5113 Super I/O chip. The IrDA interface shares one UART with serial port COM2. A control bit in the M5113 chip controls whether the UART communicates over the COM2 port or the IrDA port. See the *M5113: Enhanced Super I/O Controller Data Sheet*, available from Acer Laboratories Inc. See **www.acerlabs.com** for contact information.

Parallel Port (A22)

Figure 2-8 and Table 2-9 show the parallel port pinouts.



Notes:

See Figure 2-3 on page 2-5 for connector locations.

Figure 2-8. Parallel Port Socket (J4)

Table 2-9. Parallel Port Pin/Signal Table

Pin	Signal
1	$\overline{\text{STRB}}$
2–9	PD0–PD7
10	$\overline{\text{ACK}}$
11	BUSY
12	PE
13	SLCT
14	$\overline{\text{AFDT}}$
15	$\overline{\text{ERROR}}$
16	$\overline{\text{INIT}}$
17	$\overline{\text{SLCTIN}}$
18–25	GND

Floppy Disk Drive (E20)

The PCI CDP’s Super I/O chip provides a floppy disk controller to support the system’s floppy disk drive connector (part J6). Either a 5.25-inch or 3.5-inch floppy disk drive can be installed with a standard 34-pin connector. For details, see “Board Installation” on page 1-4.

IDE Hard Drive (L4 and M4)

The PCI CDP contains two standard 40-pin IDE connectors (parts J5 and J7). The M1498 chip provides the IDE hard drive controller. For details on how to connect a single IDE hard drive to the PCI CDP, see "Board Installation" on page 1-4.

An LED is located next to each IDE connector to indicate IDE activity. IDE devices on connector J5 can generate interrupts on IRQ14, and devices on connector J7 can generate interrupts on IRQ15. This interrupt mapping can be changed by reprogramming the chipset configuration registers.

Each connector supports one master and one slave device. If only one device is attached to an IDE connector, that device must be configured as an IDE master. If a two-position cable is used to attach two devices to a single IDE connector on the board, one of the devices must be configured as an IDE master and the other as an IDE slave. See each IDE device's documentation for configuration details.

Keyboard (O1)

The PCI CDP provides a standard AT-compatible keyboard connector (part J1) implemented via the chipset's M5402 mouse/keyboard controller chip (part U79 at location D15).

Mouse (M1)

A port is provided for a PS/2-style mouse (connector J11). This device is driven by the M5402 mouse/keyboard controller chip.

CPU Voltage Adjustment (Q15–Q16)

The CPU power supply voltage can be adjusted by moving jumper JP4 or both jumpers JP2 and JP3 on the PCI CDP. Selectable voltages are 2.5 V, 3.3 V, 3.45 V, or 5 V. Figure 2-9 shows the default configuration of the CPU voltage jumpers (set for 3.45 V).

To select either 3.3-V or 2.5-V CPU voltage, leave JP2 and JP3 set to “ADJ” and move jumper JP4 to the desired voltage.

To select 5-V operation, move *both* jumpers JP2 and JP3 to their “5 V” position.

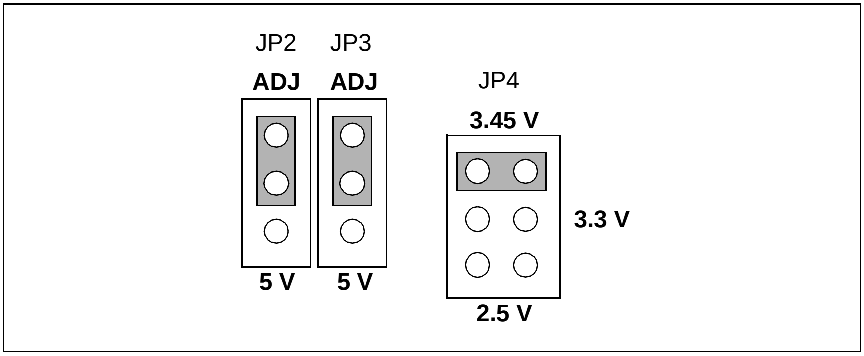
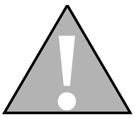


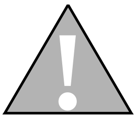
Figure 2-9. Voltage Jumper Default Configuration (Q15–Q16)



CAUTION: Jumpers JP2 and JP3 must both be placed in the same position. Positioning JP2 and JP3 differently can damage the PCI CDP.

Power Supply Connectors (N2 and P2)

The PCI CDP accepts standard PC-style motherboard power connectors to supply power to the CPU and all onboard components. To ensure proper functionality of the power module, the board's PC power supply sockets must be inserted correctly onto the board.



CAUTION: It is important that the ground wires of one connector are adjacent to the ground wires of the other. See Figure 2-10.

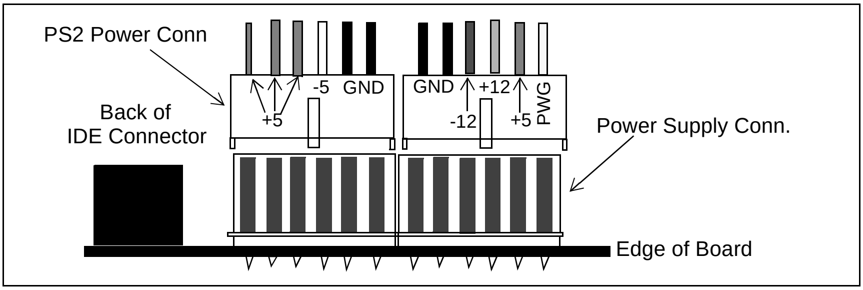


Figure 2-10. Ground Wire Connections

Reset and Interrupt Switches and Headers

Three push-button switches are provided so the user can generate RESET, SMI, and NMI events. In addition, a two-pin header is provided for the RESET signal so that an external pushbutton switch can be attached. These switches and headers are routed to the appropriate chipset signals as listed in Table 2-10.

Table 2-10. Switch Summary

Part	Signal	Description	Location in Figure 2-3 on Page 2-5	See App. B Schematics on:
SW1, JP34	PWG	Used to reset the system.	N5, K23	Sheet 17
SW2	NMI	Used to generate an NMI event.	K6	Sheet 17
SW3	EXTSMI	Used to generate an SMI event.	H11	Sheet 17

Embedded BIOS software typically enters its debugging monitor when an NMI event is generated. In addition to pressing the NMI switch, an NMI event can be caused by a PCI-bus parity error, a DRAM parity error, or an ISA-bus IOCHCK error.

Resistor Options

The PCI CDP includes a number of resistor populate/depopulate options, which are listed in Table 2-11. Many are used only as manufacturing options, but some may be useful for exploring design options or better emulating a target design.

Table 2-11. Resistor Options

Part	Signal	Description	Location in Figure 2-3 on Page 2-5	See App. B Schematics on:
R11	CLKMUL	When R11 is populated and R148 is removed, the clock multiplier for an Am486DX2-66 microprocessor is selected.	M17	Sheet 2
R58	ENRTC	When populated (the default), the M1487 chip's internal RTC is disabled and the DS1685 Y2K-compliant RTC is enabled.	I14 (back side)	Sheet 16
R59	CMPSTJ	When removed (the default), the 1X CPU-to-PCI bus frequency multiplier is selected. (1X is the only multiplier supported in this design.)	I14 (back side)	Sheet 16
R70	TURBO	When R70 is removed and R71 is populated (the default), the M1487's TURBO signal is High (asserted). This input must be enabled by software to have any effect.	I14 (back side)	Sheet 17
R71	TURBO	When R71 is populated and R70 is removed (the default), the M1487's TURBO signal is asserted. This input must be enabled by software to have any effect.	I14 (back side)	Sheet 17
R93	CLKPU2	When R93 is populated and R176 is removed, the system clock speed is 25 MHz.	J3 (back side)	Sheet 18

Table 2-11. Resistor Options (Continued)

Part	Signal	Description	Location in Figure 2-3 on Page 2-5	See App. B Schematics on:
R145	KBINHIBIT	When R145 is populated and R146 is removed (the default), the M5042 keyboard controller is enabled.	D15 (back side)	Sheet 25
R146	KBINHIBIT	When R145 is populated and R146 is removed (the default), the M5042 keyboard controller is enabled.	D15 (back side)	Sheet 25
R148	CLKMUL	When R148 is populated and R11 is removed (the default) the clock multiplier for an Am486DX4-100 or Am486DX5-133 microprocessor is selected.	M17	Sheet 2
R170	IBCSTJ	When populated (the default), the M1487's internal keyboard controller is disabled. (The M1487 internal keyboard controller function is discontinued. The M5042 is provided instead.)	I14 (back side)	Sheet 16
R176	CLKPU2	When R176 is populated and R93 is removed (the default), the system clock speed is 33 MHz.	J3	Sheet 18

Appendix A

Default Settings

This chapter lists the default settings of the Am486 microprocessor PCI customer development platform when it is shipped.

Table A-1. Default Jumper Settings

Part	Signal	Location in Figure 2-3 on Page 2-5	Default Position	Position Marking
JP2	CPUV$_{CC}$3	Q15	Pins 2–3	“ADJ”
JP3	CPUV$_{CC}$3	Q16	Pins 2–3	“ADJ”
JP4	CPUV1, CPUV2, CPUV3	R15	Pins 1–2	“3.45 V”
JP32	Boot ROM A17	C14	No connection	(No marking)
JP33	Boot ROM A18	B14	No connection	(No marking)

Appendix B

Bill of Materials and Schematics

The bill of materials for the Am486 microprocessor PCI customer development platform (CDP) begins on page B-2.

The actual schematics used to build the PCI CDP begin on page B-10.

Board Bill of Materials (BOM)

Item	Qty.	Reference	Part	Package	Description
1	119	C1, BC1, BC2, C3, BC3, C4, BC4, C5, BC5, C6, BC6, C7, BC7, C8, BC8, BC9, BC10, BC11, BC12, BC13, BC14, BC15, BC16, BC17, BC18, BC19, BC20, BC21, BC22, BC23, BC24, BC25, BC26, BC27, BC28, BC29, BC30, BC31, BC32, BC33, BC34, BC35, C36, BC36, C37, BC37, C38, BC38, C39, BC39, BC40, BC41, BC42, BC43, BC44, BC45, BC46, C47, BC47, C48, C50, C52, C65, C67, C69, C70, C71, C72, C73, C74, C75, C76, C77, C79, C80, C81, C82, C88, C89, C90, C91, C92, C93, C94, C95, C100, C105, C111, C112, C114, C115, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C156, C157, C160, C166, C167, C168, C169, C170, C171, C172, C173, C174	0.1 µF	805	RC0805, X7R, ±10%, 50 V
2	1	BT1	3 V Coin cell (socket)		KEYSTONE 103 or 106
3	14	C9, C10, C11, C12, C13, C34, C35, C83, C96, C97, C102, C103, C104, C109	0.01 µF	805	RC0805, X7R, ±10%, 50 V
4	6	C14, C28, C58, C64, C158, C159	47 pF	805	RC0805, NPO, ±5%, 50 V
5	33	C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C29, C30, C31, C32, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153	180 pF	805	RC0805, NPO, ±10%, 50 V

Notes:

An asterisk (*) indicates parts that are not populated.

Item	Qty.	Reference	Part	Package	Description
6	10	C33, C41, C42, C43, C46, C56, C57, C60, C66, C154	15 pF	805	RC0805, NPO, ±5%, 50 V
7	1	C40	1000 pF	805	RC0805, 1/8 W, ±5%, 50 V
8	2	C44, C45	39 pF	805	RC0805, NPO, ±5%, 50 V
9	4	C53, C54, C155, C161	10 pF	805	RC0805, NPO, ±5%, 50 V
10	1	C55	22 pF	805	RC0805, NPO, ±5%, 50 V
11	1	C68	6.8 µF	C-CASE	TANTALUM, C-CASE, 16 V, ±20%
12	2	C86, C78	2.2 µF	B-CASE	TANTALUM, B-CASE, 20 V, ±20%
13	23	TC2, TC3, TC9, TC11, TC12, TC13, TC14, TC15, TC16, TC17, TC18, TC19, TC22, TC23, TC24, TC25, C84, C87, C106, C107, C108, C110, C113	10 µF	C-CASE	TANTALUM, C-CASE, 16 V, ±20%
14	1	C85	1 µF	A-CASE	TANTALUM, A-CASE, 16 V, ±20%
15	2	C98, C99	33 pF	805	RC0805, NPO, ±5%, 50 V
16	1	C101	0.001 µF, 2 KV (MIN.)	TH	SPRAGUE 30GAD10
17	4	C162, C163, C164, C165	0.015 µF	805	RC0805, X7R, ±10%, 50 V
18	6	D1, D5, D6, D7, D8, D9	MMBD4148 (SOT23)	SOT-23	VISHAY MMBD4148
19	1	D10	LED (SOT23)	SURSOT-23	LUMEX SSL-LX15IC-RP
20	4	D11, D12, D13, D14	LED (SOT23)	SURSOT-23	LUMEX SSL-LX15GC-RP
21	2	D15, D17	LED (2mA, SOT23)	SOT-23	KINGBRIGHT KM-23LSGC

Notes:

An asterisk (*) indicates parts that are not populated.

Item	Qty.	Reference	Part	Package	Description
22	2	D16, D18	LED (2mA, SOT23)	SOT-23	KINGBRIGHT KM-23LEC
23	2	F1, F2	FUSE, 0.5A	1206	BUSSMAN 3216FF-500mA
24	1	HS1	HEATSINK (TO-220)		THERMALLOY ML32
25	7	JP2, JP3, JP29, JP30, JP31, JP32, JP33	HEADER 3X1	TH-1X3	1X3 HEADER; 0.025” SQ. POST AMP 87224-3
26	1	JP4	HEADER 3X2	TH-2X3	1X3 HEADER; 0.025” SQ. POST AMP 103186-3
27	1	JP34	HEADER 2X1	TH-1X2	1X2 HEADER; 0.025” SQ. POST AMP 87224-2
28	1	J1	KYBD CONN	TH	AMP 212044-1
29	2	J2, J3	PWR-CN6	TH	MOLEX 15-48-0106
30	1	J4	Parallel Port	DB25	AMP 745967-7
31	2	J7, J5	CNN-40C	TH-2X20-SHRD	2X20 HEADER; SHRD AMP 103308-8
32	1	J6	CNN-34C	TH-2X17-SHRD	2X17 HEADER; SHRD AMP 103308-7
33	2	J8, J9	SERIAL PORT	DB9	AMP 745410-1
34	1	J10	AMP RJ45A	TH	AMP 555153-1
35	1	J11	MOUSE_CON	TH	AMP 750329-2
36	1	LS1	SPEAKER		ISL PROD. INTL. ISL-8032VT
37	9	L1, L2, L3, L4, L5, L6, L7, L8, L9	FB	RC1206	MURATA ERIE BLM32A07
38	10	MT1, MT2, MT3, MT4, MT5, MT6, MT7, MT8, MT9, MT10	Mounting Hole		
39	1	P31	COND60	AMPMOD 50, 1X30, R-ANG	AMP 104069-7
40	2	P35, P48	HEADER2X5; SHRD	TH-1X5-SHRD	2X5 HEADER; SHRD AMP 103308-1

Notes:

An asterisk (*) indicates parts that are not populated.

Item	Qty.	Reference	Part	Package	Description
41	11	P36, P38, P39, P40, P41, P42, P43, P44, P45, P46, P47	HP CONN	TH-1X10-SHRD	3M:2520-6003UB or AMP 103308-5
42	1	Q1	MMBT3906 (SOT23)	SOT-23	VISHAY MMBT3906
43	2	Q4, Q2	MMBT3904 (SOT23)	SOT-23	VISHAY MMBT3904
44	1	Q5	TIP127	TO-220	MOTOROLA TIP127
45	9	RN1, RN2, RN3, RN4, RN8, RN9, RN10, RN11, RN12	33-8B		CTS 743 08-3 330 J TR
46	7	RN5, RN6, RN7, RN13, RN14, RN15, RN16	22-8B		CTS 743 08-3 220 J TR
47	12	RP1, RP2, RP5, RP6, RP7, RP12, RP14, RP16, RP17, RP18, RP19, RP20	10 K-10P	SIP10	CTS 770 10 1 103 SP
48	2	RP4, RP3	1 K-10P	SIP10	CTS 770 10 1 102 SP
49	6	RP8, RP9, RP10, RP11, RP15, RP21	4.7 K-10P	SIP10	CTS 770 10 1 472 SP
50	1	RP13	330-8P	SIP8	CTS 770 8 1 331 SP
51	19	R3, R4, R5, R13, R19, R49, R50, R52, R61, R64, R68, R76, R77, R91, R104, R131, R141, R142, R175	10 K	805	RC0805, 1/8 W, ±5%, 50 V
52	17	R6, R20, R21, R34, R58, R78, R85, R103, R105, R118, R130, R134, R170, R173, R174, R177, R178	1 K	805	RC0805, 1/8 W, ±5%, 50 V
53	5	R7, R8, R27, R81, R124	33	805	RC0805, 1/8 W, ±5%, 50 V
54	1	R11	*10 K	805	RC0805, 1/8 W, ±5%, 50 V
55	6	R14, R15, R16, R17, R18, R147	22	805	RC0805, 1/8 W, ±5%, 50 V
56	11	R22, R31, R35, R36, R38, R41, R42, R54, R99, R100, R101	10	805	RC0805, 1/8 W, ±5%, 50 V
57	1	R23	27.4 K, 1%	805	RC0805, 1/8 W, ±1%, 50 V

Notes:

An asterisk (*) indicates parts that are not populated.

Item	Qty.	Reference	Part	Package	Description
58	1	R25	25.5 K, 1%	805	RC0805, 1/8 W, ±1%, 50 V
59	1	R26	15.8 K, 1%	805	RC0805, 1/8 W, ±1%, 50 V
60	10	R28, R94, R97, R135, R136, R137, R138, R156, R158, R160	330	805	RC0805, 1/8 W, ±5%, 50 V
61	1	R29	15.0 K, 1%	805	RC0805, 1/8 W, ±1%, 50 V
62	4	R30, R65, R139, R140	100	805	RC0805, 1/8 W, ±5%, 50 V
63	15	R33, R47, R57, R119, R120, R121, R122, R123, R127, R148, R163, R165, R167, R169, R176	0	805	RC0805, 1/8 W, ±5%, 50 V
64	9	R39, R44, R45, R75, R90, R92, R106, R171, R172	4.7 K	805	RC0805, 1/8 W, ±5%, 50 V
65	1	R48	51 K	805	RC0805, 1/8 W, ±5%, 50 V
66	1	R59	*1 K	805	RC0805, 1/8 W, ±5%, 50 V
67	5	R62, R63, R149, R150, R151	270	805	RC0805, 1/8 W, ±5%, 50 V
68	2	R70, R146	*2.2 K	805	RC0805, 1/8 W, ±5%, 50 V
69	9	R71, R80, R95, R96, R98, R145, R157, R159, R161	470	805	RC0805, 1/8 W, ±5%, 50 V
70	1	R79	10M	805	RC0805, 1/8 W, ±5%, 50 V
71	1	R93	*4.7 K	805	RC0805, 1/8 W, ±5%, 50 V
72	1	R102	47	805	RC0805, 1/8 W, ±5%, 50 V
73	1	R107	100, 1%	805	RC0805, 1/8 W, ±1%, 50 V
74	2	R108, R109	49.9, 1%	805	RC0805, 1/8 W, ±1%, 50 V

Notes:

An asterisk (*) indicates parts that are not populated.

Item	Qty.	Reference	Part	Package	Description
75	4	R110, R111, R112, R113	75, 1%	805	RC0805, 1/8 W, ±1%, 50 V
76	3	R114, R115, R117	1.00 K, 1%	805	RC0805, 1/8 W, ±1%, 50 V
77	1	R116	22 K, 1%	805	RC0805, 1/8 W, ±1%, 50 V
78	4	R152, R153, R154, R155	1.5 K	805	RC0805, 1/8 W, ±5%, 50 V
79	4	R162, R164, R166, R168	*0	805	RC0805, 1/8 W, ±5%, 50 V
80	3	SIMM1, SIMM2, SIMM0	SIMM72		AMP 822030-3
81	2	SLT1, SLT2	PCI Slot		AMP 145154-4
82	2	SL1, SL2	ISA AT Connector		AMP 645169-3
83	3	SW1, SW2, SW3	PBNO		C&K KT11P2SM
84	4	TC1, TC4, TC7, TC10	47 µF	D-CASE	TANTALUM, D-CASE, 16 V, ±20%
85	4	TC5, TC6, TC20, TC21	10 µF	D-CASE	TANTALUM, D-CASE, 25 V, ±20%
86	1	TC8	100 µF	E-CASE	TANTALUM, E-CASE, 16 V, ±20%
87	1	T1	PE68515		PULSE ENGR. PE-68515
88	1	U1	74F245	SOL20	SIGNETICS 74F245D
89	1	U5	M1489	PQFP208	ALi M1489
90	1	U6	LP2951	SO8	NATIONAL LP2951CM
91	4	U7, U8, U9, U10	128 Kx8-15	SOJ32(0.3”/0.4”)	128 Kx8, 15 ns, Corner Vcc/GND Pins, SOJ32
92	1	U11	32 Kx8-15	SOJ28(.3”)	32 Kx8, 15 ns, Corner Vcc/GND Pins, 0.3”SOJ28
93	1	U14	Am29F010-90	DIP32(0.6”)(SOCKET)	AMD Am29F010-90PC
94	1	U15	74F04	SO14	SIGNETICS 74F04D

Notes:

An asterisk (*) indicates parts that are not populated.

Item	Qty.	Reference	Part	Package	Description
95	1	U17	IMI SC464	SSOP28	INTL. MICROCKTS. INC. IMISC464AYB
96	1	U21	M1487	PQFP160	ALi M1487
97	1	U22	DS1685-5	DIP24(0.650”)	DALLAS SEMI. DS1685-5
98	2	U24, U82	74F08	SO14	SIGNETICS 74F08D
99	1	U25	Am486 Microprocessor, PGA	PGA169	AMD (AMP SOCKET1 916504-2)
100	11	U26, U28, U30, U31, U32, U36, U38, U40, U47, U49, U70	74ABT16244	SSOP48	SIGNETICS 74ABT16244ADL
101	1	U42	74ABT244	SOL20	SIGNETICS 74ABT244D
102	1	U43	M5113A	PQFP100	ALi M5113A
103	1	U44	TFDS6000	SMT	TEMIC TFDS6000D
104	2	U46, U45	RS232-5V	SSOP28	LINEAR TECH LTC1349CG
105	1	U51	Am79C972 (PQR160)	PQR160	AMD Am79C972KC
106	1	U52	LXT970QC	MQFP64	LEVEL ONE LXT970QC
107	1	U53	MC33269DT-3.3	DPAK	MOTOROLA MC33269DT-3.3
108	1	U54	NM93C46N	DIP8	NATIONAL NM93C46N
109	1	U55	MACH221	PQFP-100	AMD MACH221SP-7
110	9	U56, U61, U62, U63, U64, U65, U66, U67, U68	29F800-55 TSOP48	TSOP48	AMD AM29F800BT-55EC
111	2	U60, U80	PALCE22V10_PLCC (5ns)	PLCC28	AMD PALCE22V10H-5JC
112	1	U69	74ABT373	SOL20	SIGNETICS 74ABT373AD
113	1	U71	74ABT16245	SSOP48	SIGNETICS 74ABT16245BDL
114	4	U72, U73, U74, U75	Hex Display	TH	TI TIL311

Notes:

An asterisk (*) indicates parts that are not populated.

Item	Qty.	Reference	Part	Package	Description
115	1	U77	74F32	SO14	SIGNETICS 74F032D
116	1	U78	74F06	SO14	SIGNETICS 74F06D
117	1	U79	M5042	PLCC44	ALi M5042
118	1	U81	NM93C66M8	SO8	NATIONAL NM93C66M8
119	1	U83	74F14	SO14	SIGNETICS 74F14D
120	1	U84	74ABT125	SO14	Signetics 74ABT125D
121	1	Y1	24 MHz_SMD		ECLIPTEK ECSMA-24.00MTR
122	1	Y2	14.318 MHz_SMD		ECLIPTEK ECSMAT-14.318MTR
123	2	Y4, Y6	32.768 KHz_SMD		ECLIPTEK ECPSM29T-32.768KTR
124	1	Y5	25 MHz_SMD		ECLIPTEK ECSMA-25.000MTR
127	1	XU14	DIP32(0.6”) SOCKET		SAMTEC ICA-632-SGG
128	1	XBT1	3.3 V LITHIUM COINCELL		TOSHIBA CR2032
129	1	U25-HS	FANSINK FOR CPU		THERMALLOY 2321B-TCM-42S-PF17
130	5	XXX	JUMPERS (0.1”)	FOR 0.025” SQ. POSTS	

Notes:

An asterisk (*) indicates parts that are not populated.

Schematics

The schematics that follow are the actual CAD schematics used to build the PCI CDP. These schematics are useful for understanding and modifying the PCI CDP. Because the development platform is based on a particular chipset and incorporates many different possible design options, actual Am486 microprocessor-based designs might be considerably different.

Am486 Microprocessor PCI Customer Development Platform

Am486 Microprocessor Development System With PCI Expansion and On-Board Am79C972 100MB/s Ethernet Controller

Table of Contents

Rev 1.0: Original design

Rev 1.1: Minor modifications after Design Review

Rev 1.2: Added External 8042 Style Keyboard Controller (SH24)
Removed Support for M1487 Internal KBC (SH15)
Removed Keyboard Interface From Clock Page (SH17)
Changed design name to Am486PCI C.D.P.

Rev 1.3: Added Extra Bypass Capacitors (SH5 & SH14 & SH15 & SH17)
Swapped Around Some Signals Within Resistor Networks (SH6 & SH20)
Renamed MCLK1 net to M_CLK1 (SH24)
Added 0-ohm resistor to make pin 10 & 11 pullup work (SH17)
Added Pin to HS1 for NetLister (SH3)
Fixed Error in 3.3V Regulator Circuit (SH12)

Rev 1.4: Rearranged Clock Nets to Facilitate Routing (SH17)
Changed Some Components to Standard Values
(50ohm to 49.9ohm, 1% on SH 13 and 40pF to 39pF,
5% on SH19)

Rev 2.0: Changed SIP resistor packs to 10-pin (SH2, SH3, SH11, SH15, SH16, SH17, SH19, SH20 & SH21)
Changed 330ohm SIP Resistor Pack to 8-pin (SH19)

SH3: Added diagram to correct Power Connector Footprint

SH4 & 5: Broke CPU Logic Analyzer Headers into 2 pages
Added PAL to gnerate CPU A0 and A1 and also generate a Logic Analyzer Qualify signal
Buffered BE[0..3], RDY#, BRDY#, and ADS# through the new PAL

SH9: Added better explanation of EIP Flash memory operation

SH11: Added configuration information for PCI slots
Removed circuit to generate PCI PERR# to cause
M1487 to assert NMI to Am486 microprocessor

SH13: Added a 4K serial EEPROM for user parameters and mux. circuit to daisy chain it off the 1K device.
'972 E/net device loads its configuration from 1K SEEPROM.
CLKCNTL signal from M1487 used to select 1K or 4K SEEPROM.

SH14: Swapped R107 and R109; R109 is 49.9ohm, 1%
Fixed wiring error on crystal

SH15: Added 5 more 0.1uF bypass capacitors for new chips ('F14, 'ABT125, 22V10, 'F08, 'C66)

SH16: Fixed wiring error on crystal
Fixed wiring error in generation of low-active reset signal RSTDRV#
Removed unused inverter (used on SH24)
Changed net on NMI pin to 1487NMI for use in new circuit
Changed R58 to be a populated component

Rev 2.0 (continued): SH17: Added jumpers to allow mulitple BIOS images in a single Flash ROM device
Removed 1 diode from VBAT generation circuit
Added new NMI generation circuit and spare 'F14 gates
Added jumper for external RESET# pushbutton

SH18: Fixed wiring error on crystal
Removed MCLK1 net (16MHz) and rewired MCLK2 to drive all 33MHz clock nets
Removed CLKCNTL signal from DOZE# pin of U17

SH20: Removed unneeded 0-ohm resistors from Super I/O chip
Fixed wiring error on crystal
Added 'ABT125 buffer to drive serial port LEDs

SH22: MACH device outputs changed for new ISA Flash support

SH23: Changed ISA Flash to 1MByte (512Kx16)

SH24: Removed unneeded logic from RTC interface
Added inverter to generate proper CS# for RTC chip
Fixed wiring error on crystal
Grounded U22-pin 22
Removed 1 unused OR gate for use on SH17

SH25: Switched mouse connector to verticle type
Changed 'F06 symbol to show o/c

Rev 2.1: Updated revision level and prototype warning on all sheets

SH17: Modified ROM jumpers to allow mulitple BIOS images in a single Flash ROM
device and support 256K or 512K BIOS for non-PC applications

SH22: Added XBUSCSJ signal to Mach device so it does not respond when Am486
fetches the reset vector at FFFF FFF0

SH14 &15 &20: Connected pins 1 and 2 on all LEDs for greater
purchasing/manufacturing flexibility

Note: Unless otherwise noted all logic operates off a 5V power supply

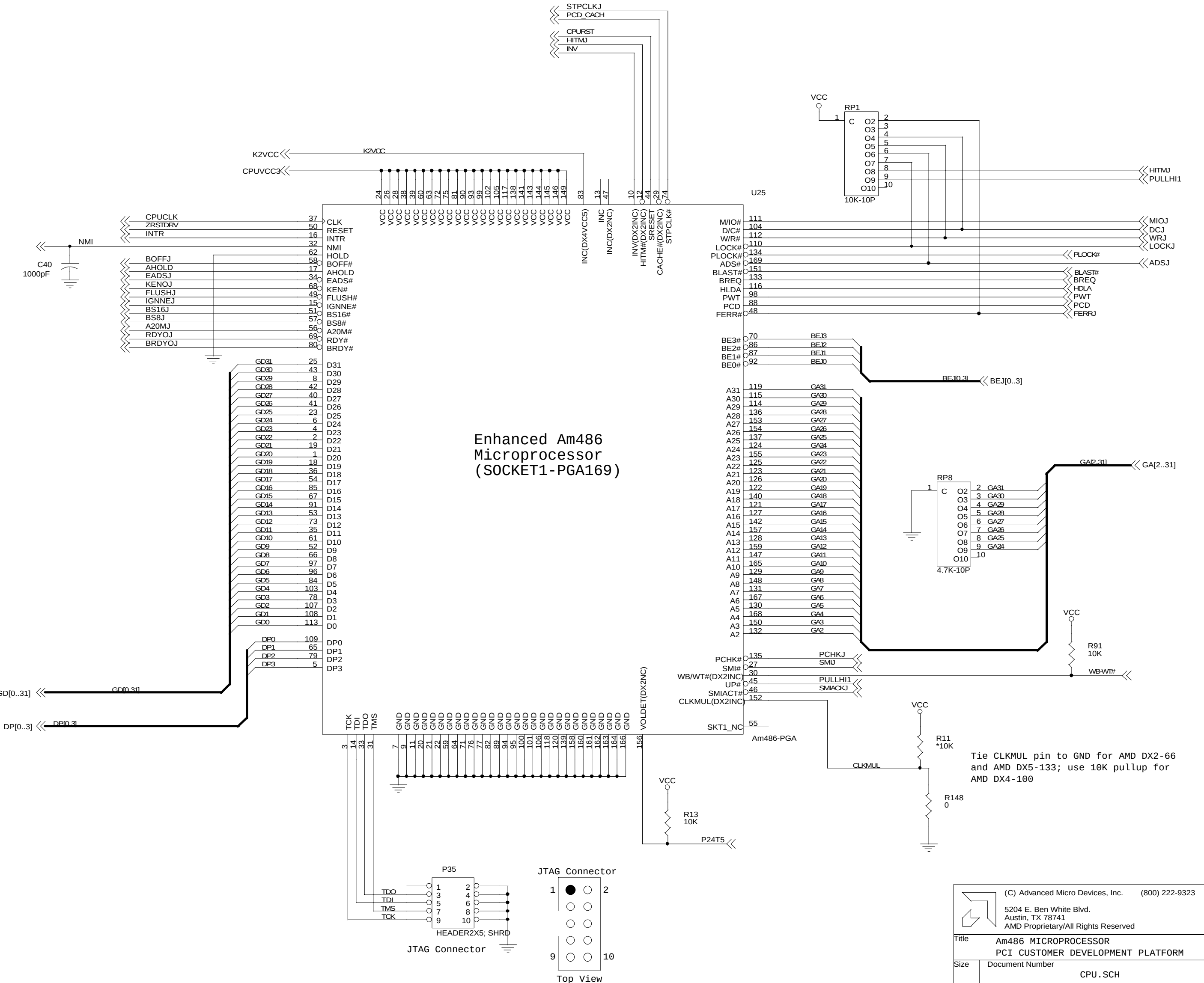
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

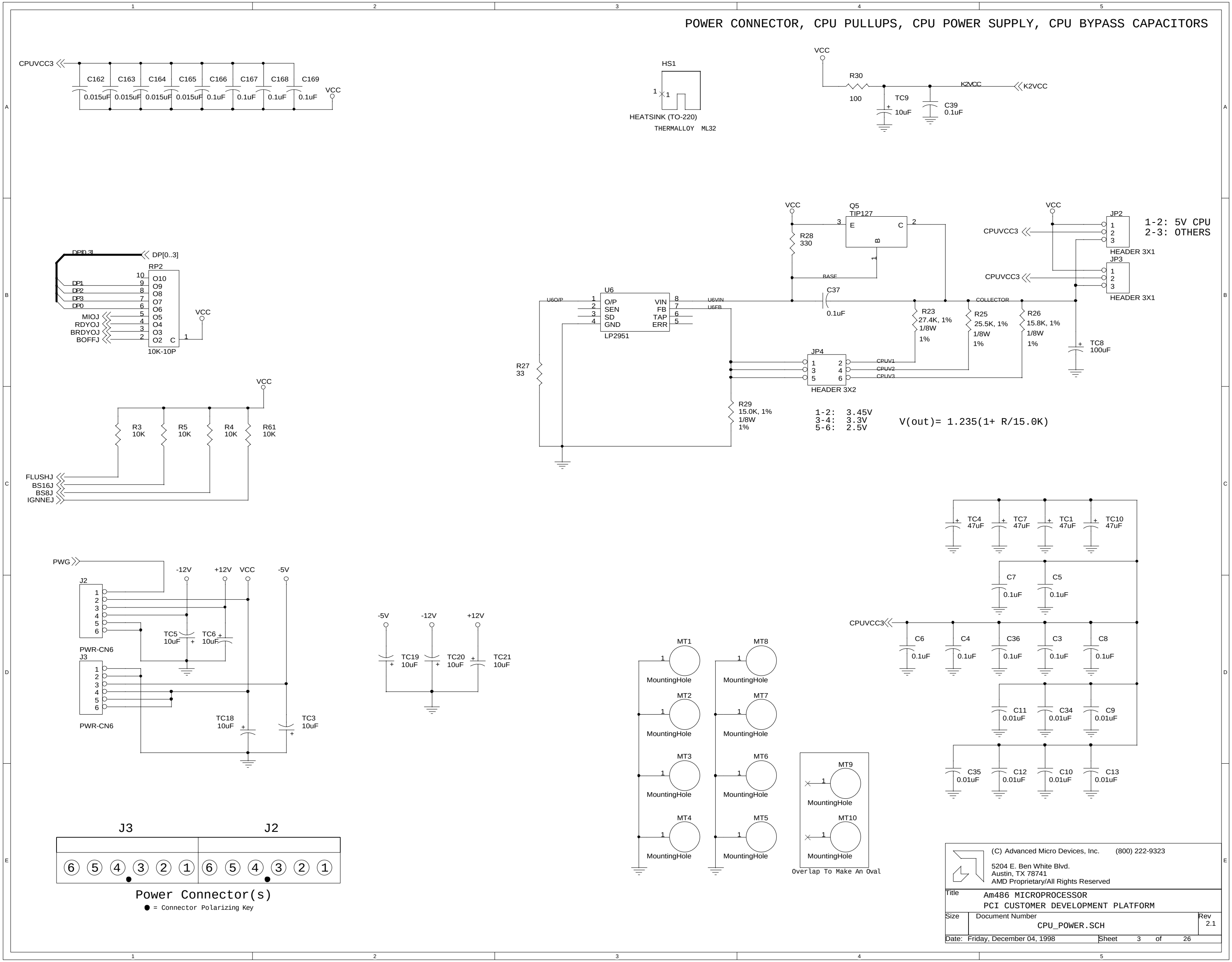
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	
Document Number	COVER.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	1 of 26

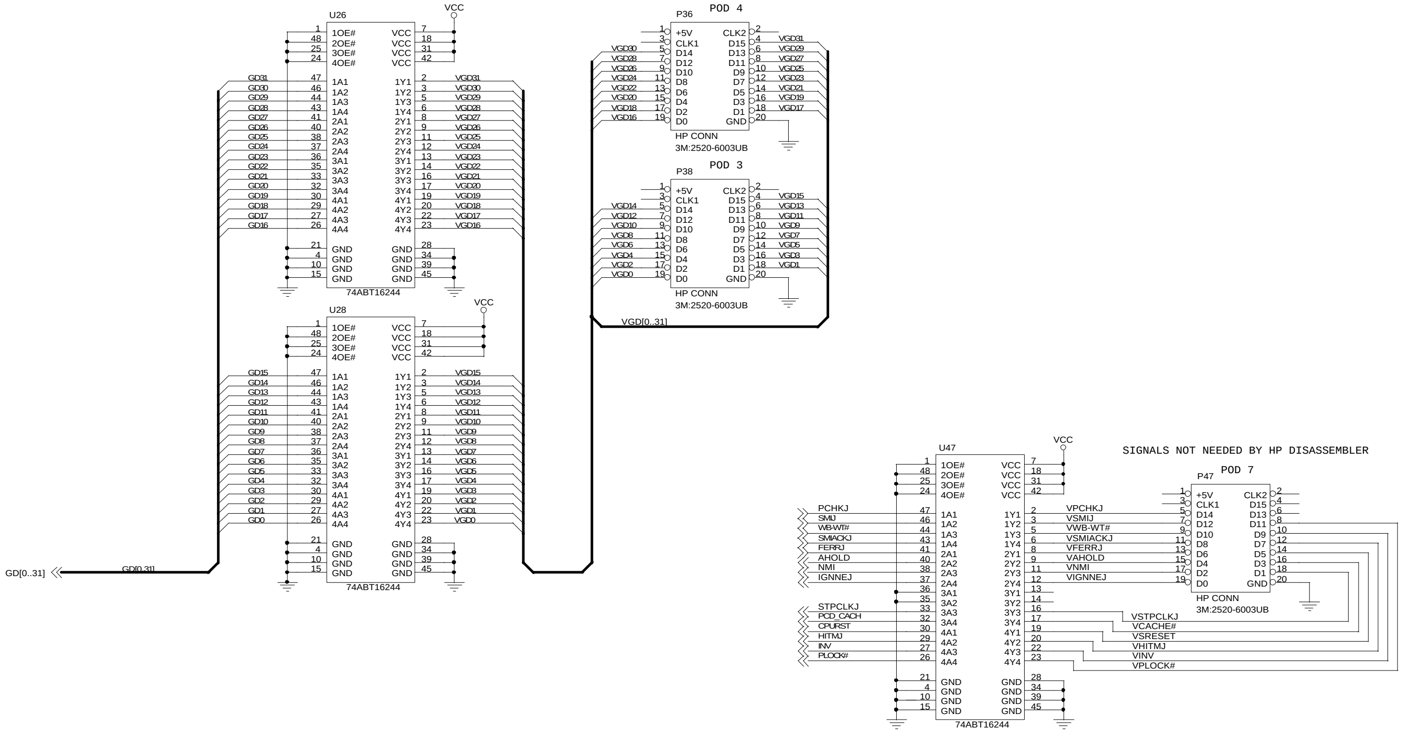
Am486 MICROPROCESSOR, PULLUPS, AND JTAG INTERFACE



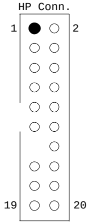
(C) Advanced Micro Devices, Inc.	(800) 222-9323
5204 E. Ben White Blvd. Austin, TX 78741 AMD Proprietary/All Rights Reserved	
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	CPU.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 2 of 26


POWER CONNECTOR, CPU PULLUPS, CPU POWER SUPPLY, CPU BYPASS CAPACITORS
CPUVCC3
C162 C163 C164 C165 C166 C167 C168 C169
0.015uF 0.015uF 0.015uF 0.015uF 0.1uF 0.1uF 0.1uF 0.1uF
VCC
HS1
HEATSINK (TO-220)
THERMALLOY ML32
R30 100
TC9 10uF
C39 0.1uF
K2VCC
DP[0..3]
RP2
10K-10P
DP1 DP2 DP3 DP0
MIOJ RDYOJ BRDYOJ BOFFJ
O10 O9 O8 O7 O6 O5 O4 O3 O2 C
R3 10K
R5 10K
R4 10K
R61 10K
FLUSHJ
BS16J
BS8J
IGNNEJ
Q5 TIP127
R28 330
BASE
U6 LP2951
O/P SEN SD GND VIN FB TAP ERR
U6O/P U6VIN U6FB
C37 0.1uF
R27 33
R23 27.4K, 1% 1/8W 1%
R25 25.5K, 1% 1/8W 1%
R26 15.8K, 1% 1/8W 1%
COLLECTOR
TC8 100uF
JP2 HEADER 3X1
JP3 HEADER 3X1
1-2: 5V CPU
2-3: OTHERS
JP4 HEADER 3X2
CPUV1 CPUV2 CPUV3
R29 15.0K, 1% 1/8W 1%
1-2: 3.45V
3-4: 3.3V
5-6: 2.5V
V(out)= 1.235(1+ R/15.0K)
TC4 47uF
TC7 47uF
TC1 47uF
TC10 47uF
C7 0.1uF
C5 0.1uF
C6 0.1uF
C4 0.1uF
C36 0.1uF
C3 0.1uF
C8 0.1uF
C11 0.01uF
C34 0.01uF
C9 0.01uF
C35 0.01uF
C12 0.01uF
C10 0.01uF
C13 0.01uF
PWG
J2 PWR-CN6
J3 PWR-CN6
-12V +12V VCC -5V
TC5 10uF
TC6 10uF
TC18 10uF
TC3 10uF
TC19 10uF
TC20 10uF
TC21 10uF
MT1 MT2 MT3 MT4 MT5 MT6 MT7 MT8 MT9 MT10
MountingHole
Overlap To Make An Oval
J3 J2
6 5 4 3 2 1 6 5 4 3 2 1
Power Connector(s)
● = Connector Polarizing Key
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved
Title
Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM
Size
Document Number
CPU_POWER.SCH
Rev 2.1
Date: Friday, December 04, 1998
Sheet 3 of 26

BUFFERS AND LOGIC ANALYZER HEADERS FOR CPU SIGNALS



HP Conn.



Top View

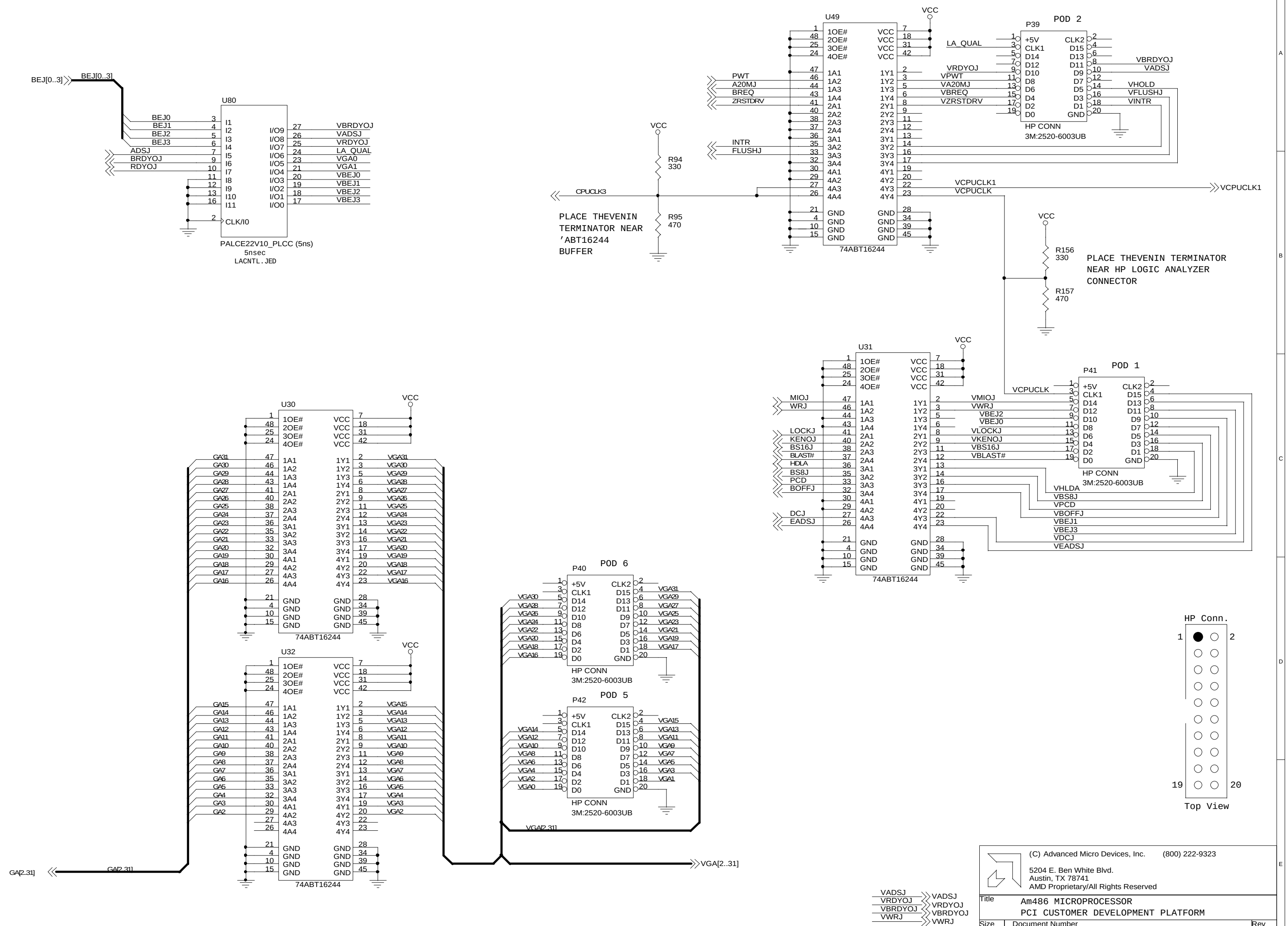
Using Logic Analyzer Headers:

Clock the analyzer off the clock signal on P41 (POD1)

Qualify the clock using the LA_QUAL signal on P39 (POD2)
This qualification signal is asserted (1) when ADS#, RDY# or BRDY# is asserted on the Am486 Microprocessor bus.
Thus cycles where valid address or data information is not transferred can be filtered out when needed
Signals are arranged on the LA Headers to work with the HP Disassembler for the 16500 analyzer

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	CPU_VIS1.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	4 of 26

BUFFERS AND LOGIC ANALYZER HEADERS FOR CPU SIGNALS, AND PAL TO AID LOGIC ANALYZER USE

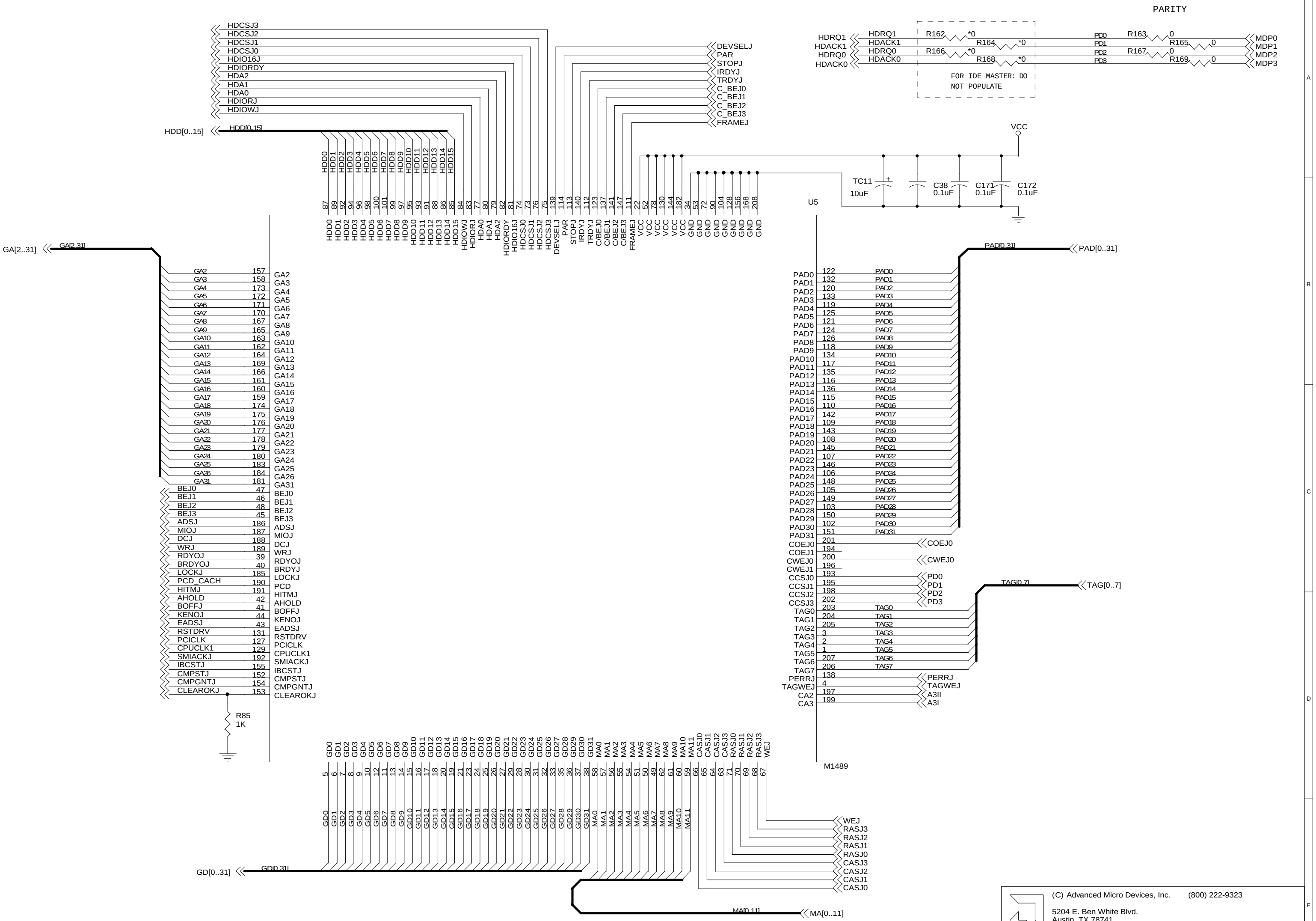


(C) Advanced Micro Devices, Inc. (800) 222-9323

5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: CPU_VIS2.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	5 of 26

FINALi M1489 INTERFACE

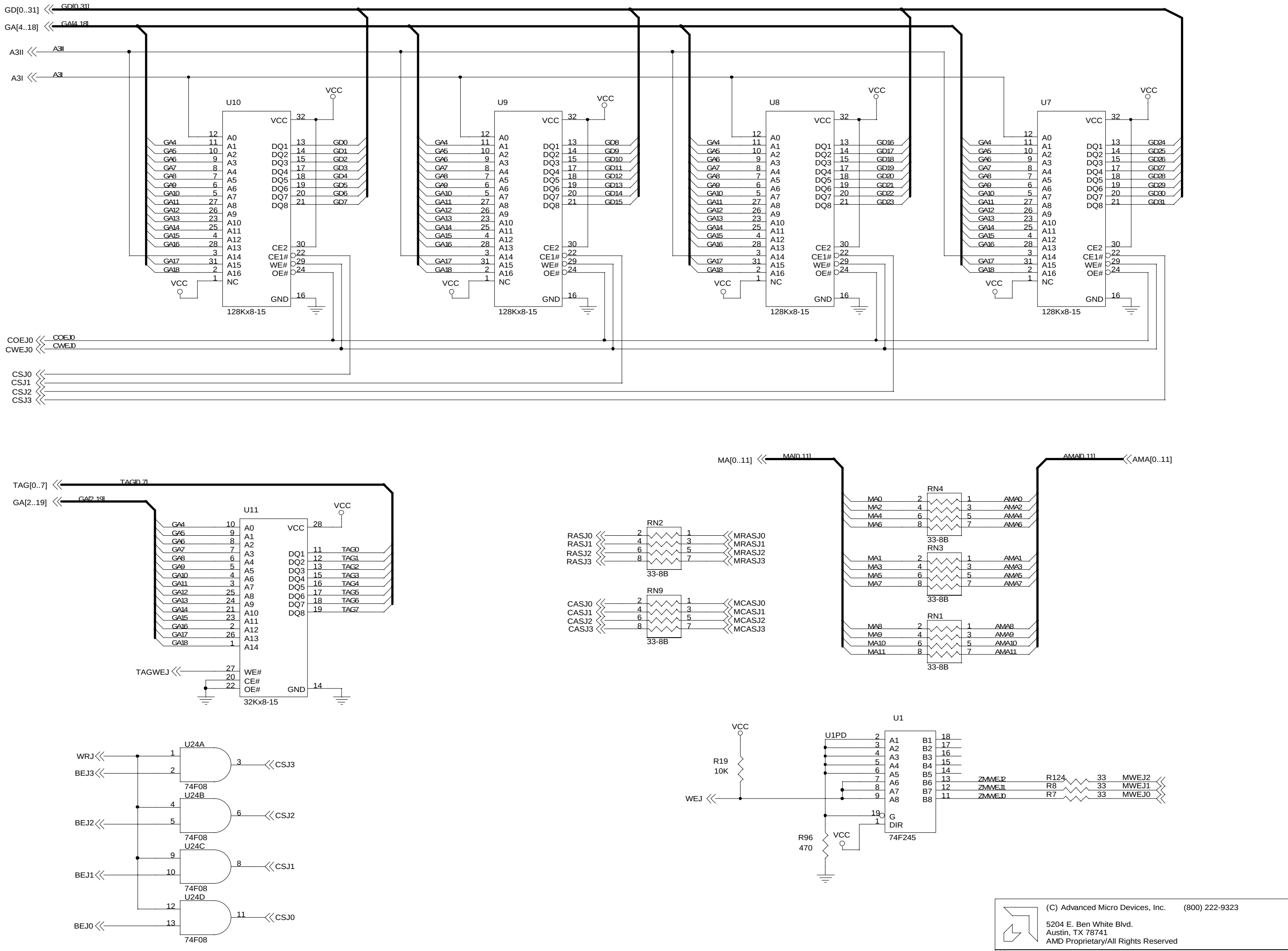


(C) Advanced Micro Devices, Inc. (800) 222-9323

5204 E. Ben White Blvd.
Austin, TX 78741

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: M1489.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	6 of 26

L2 CACHE TAG AND DATA SRAMS AND BYTE CONTROL; DRAM SERIES TERMINATION AND WE* FANOUT

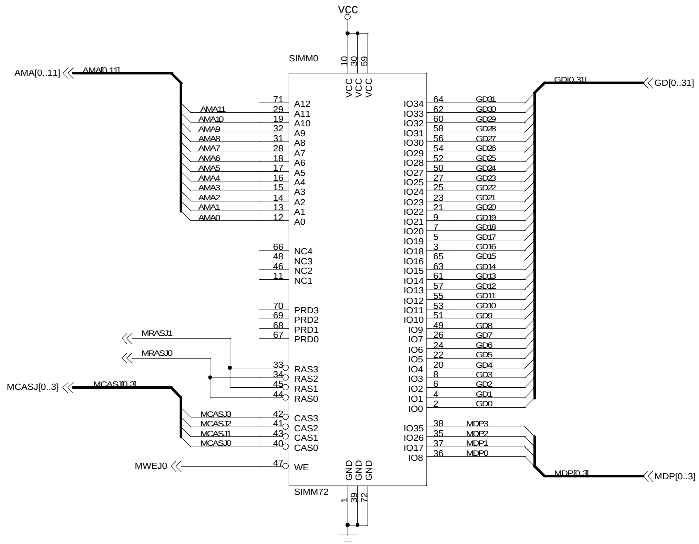


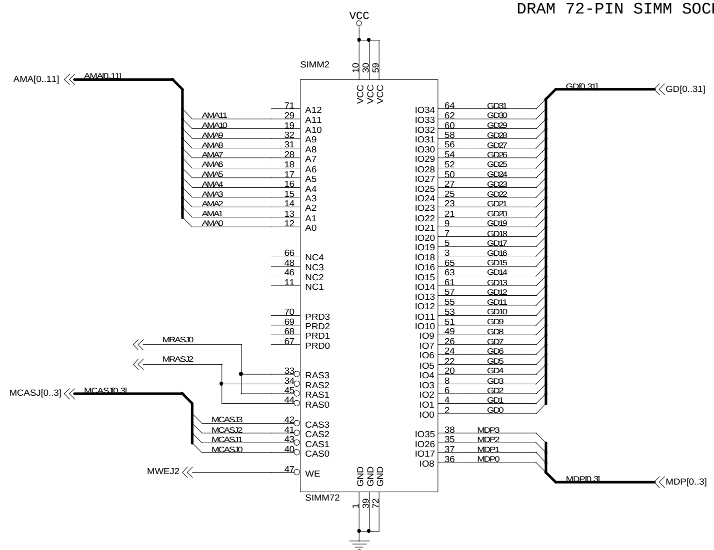
(C) Advanced Micro Devices, Inc. (800) 222-9323

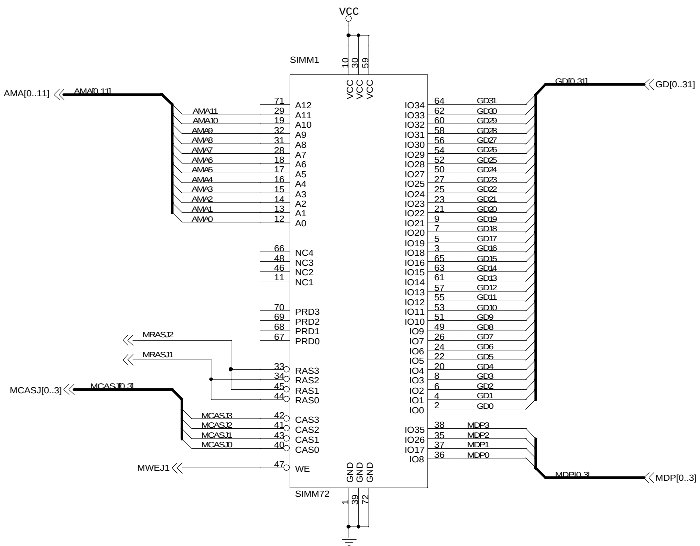
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: L2_CACHE.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	7 of 26

DRAM 72-PIN SIMM SOCKETS







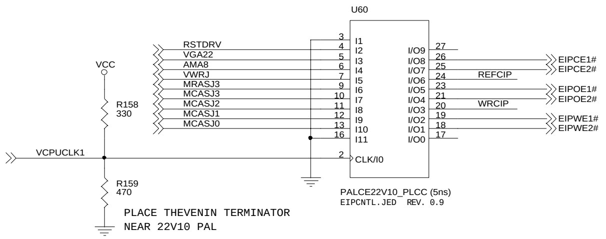
SIMM SOCKET POPULATION CHART

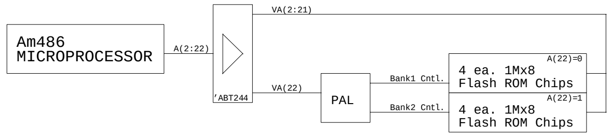
SIMM0	SIMM1	SIMM2
SINGLE BANK	SINGLE BANK	SINGLE BANK
DOUBLE BANK	SINGLE BANK	X

SIMMS CAN BE SINGLE BANK OR DOUBLE BANK, USING 1Mbit, 4Mbit, or 16Mbit DRAM CHIPS. POPULATE SIMM SOCKETS AS SHOWN IN THIS CHART.

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number: SIMM_SKTS.SCH	Rev 2.1
Date: Friday, December 04, 1998	Sheet 8 of 26	

EIP FLASH MEMORY CONTROLLER





CPU Address Bit A(22) Used As Flash Bank Select

Makes 2 banks of 1Mx32 Flash ROM appear as 1 bank of 2Mx32 DRAM (70ns, FPM) to M1489 Memory Controller. Program M1489 for 2Mx8 (11/10) DRAM chips. MA8 (CPU A22) used as Flash ROM Bank Select when RAS3# asserted by M1489 Memory Controller.

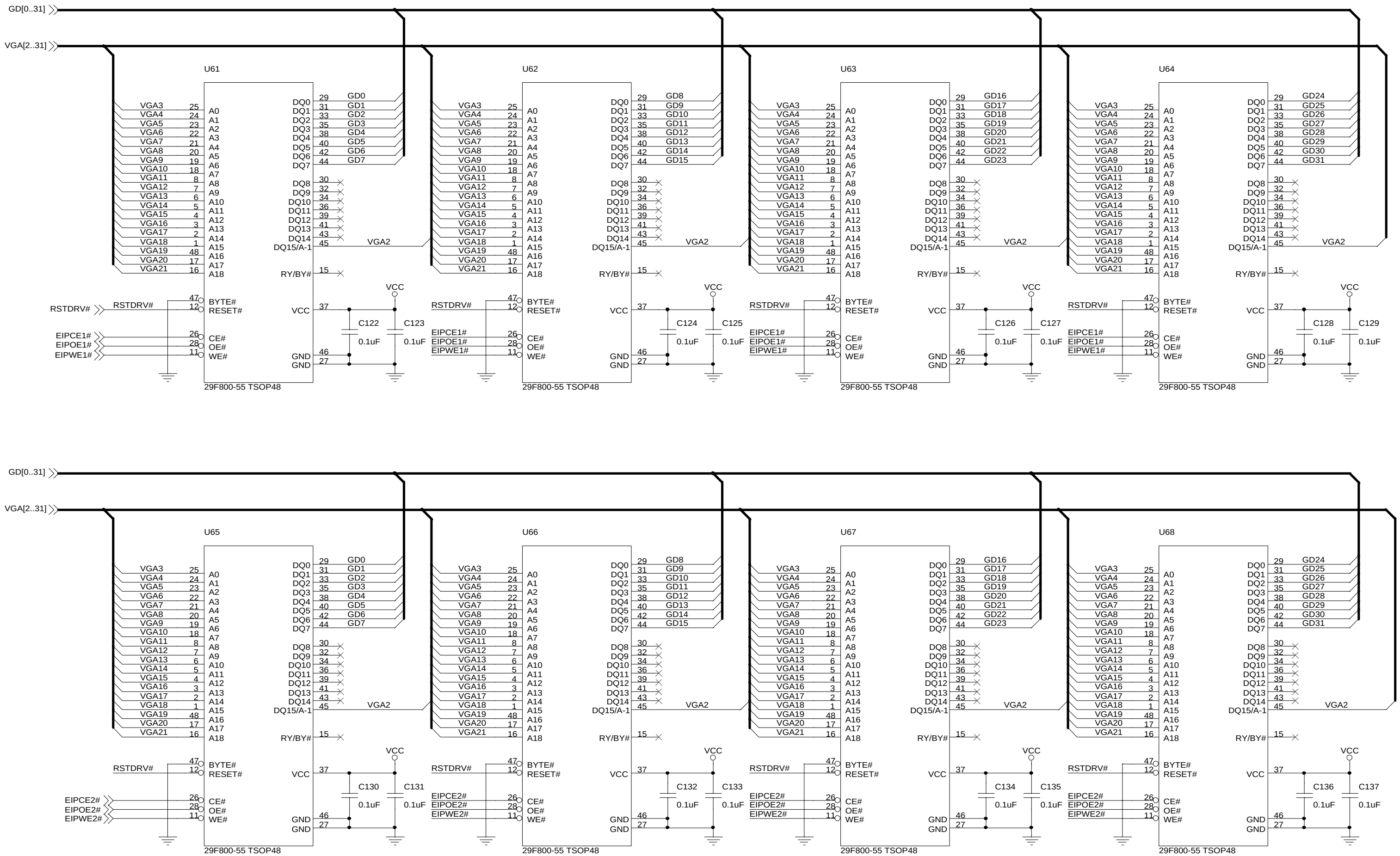
Limitations and Operation of the EIP Interface:

- Access as 32-bits wide always
- Supports burst Read Cycles or single-beat Read Cycles
- Supports single-beat Write Cycles only; no back-to-back Write Cycles
- Compatible with CAS-before-RAS Refresh Cycles only
- Set M1489 Memory Controller to "Fast" for proper operation, even if installed DRAM is 60ns and can run at the "Fastest" setting
- Flash chip A0 pin tied to Am486 Microprocessor A2 pin, so multiply desired Flash chip address by 4h to find Am486 Microprocessor address needed to access the desired memory cell (ex: Flash Chip AAAh accessed by Am486 Microprocessor at 2AA8h)
- EIP Flash Array start address moves, depending on how much DRAM is installed (ex: 48MByte DRAM puts EIP start address at 48MB or 3000000h for first bank of Flash ROMs and 3400000h start address for second bank of Flash ROMs
- Uses 29F800T, 55ns devices in "Byte" mode
- Accessable from Am486 Microprocessor only; not accessable from PCI Bus Masters
- Uses fourth DRAM bank of M1489 Memory Controller

(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	EIP_MEM1.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	9 of 26

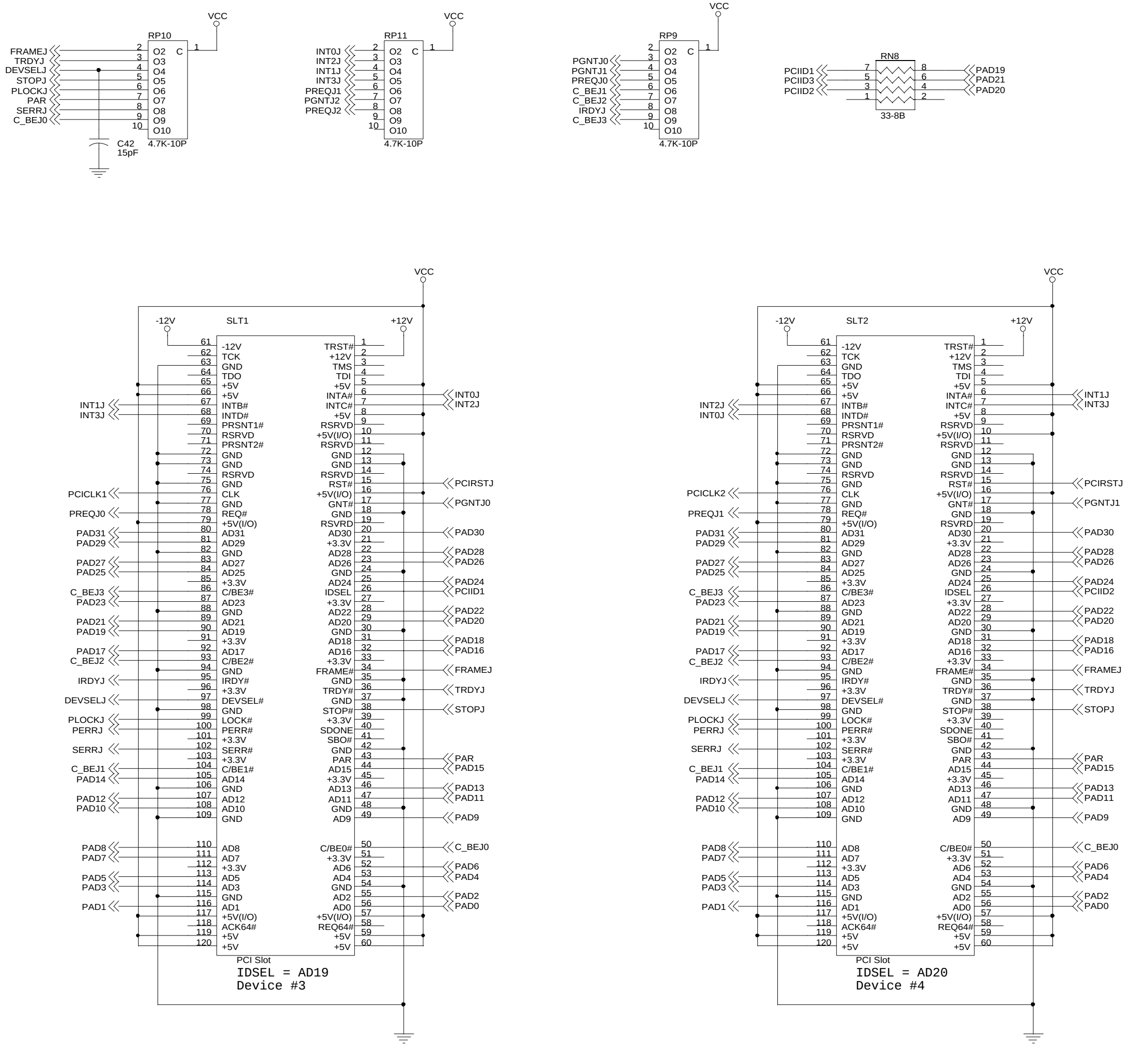
EIP FLASH MEMORY ARRAY



Title: Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM

Size	Document Number	Rev
	EIP_MEM2.SCH	2.1

Date: Friday, December 04, 1998 — Sheet 10 of 26



PCIBus INT	Slot1	Slot2	Ethernet
INT0#	INTA#	INTD#	
INT1#	INTB#	INTA#	
INT2#	INTC#	INTB#	INTA#
INT3#	INTC#	INTC#	

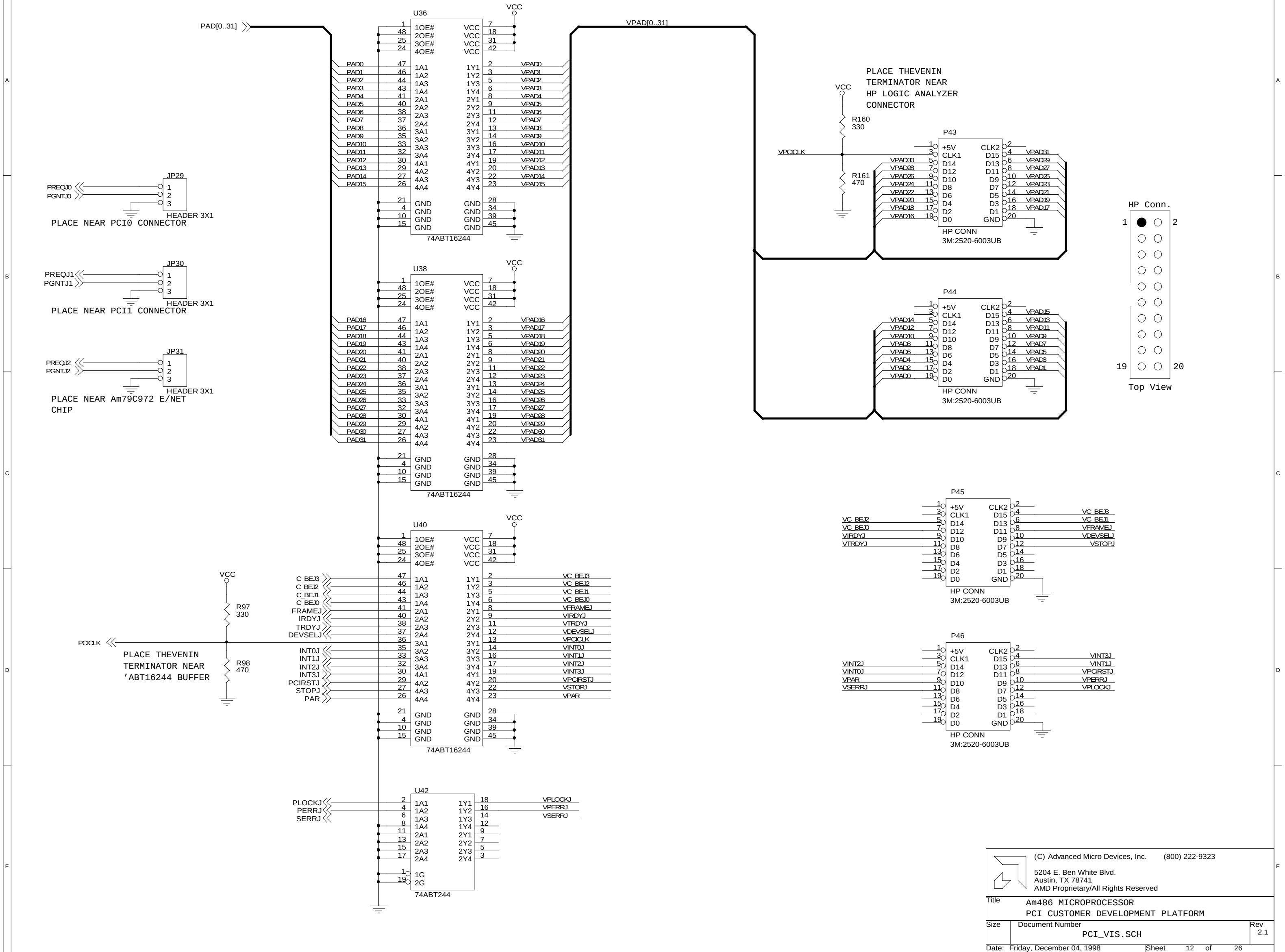
5204 E. Ben White Blvd.
Austin, TX 78741

Title: Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM

Size | Document Number: PCI_CONN.SCH | Rev 2.1

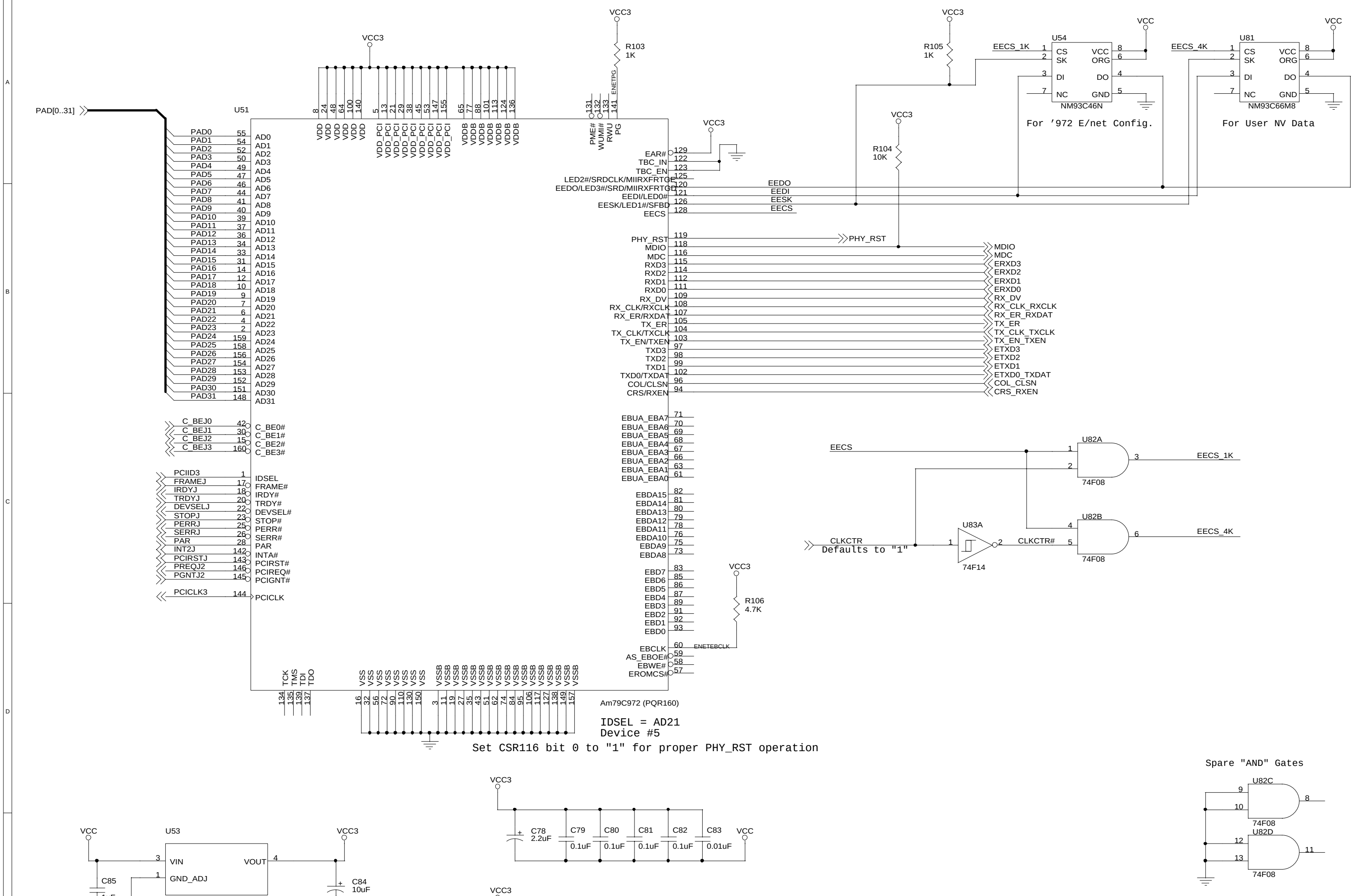
Date: Friday, December 04, 1998 | Sheet 11 of 26

BUFFERS AND LOGIC ANALYZER HEADERS FOR PCI BUS



Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	PCI_VIS.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	12 of 26

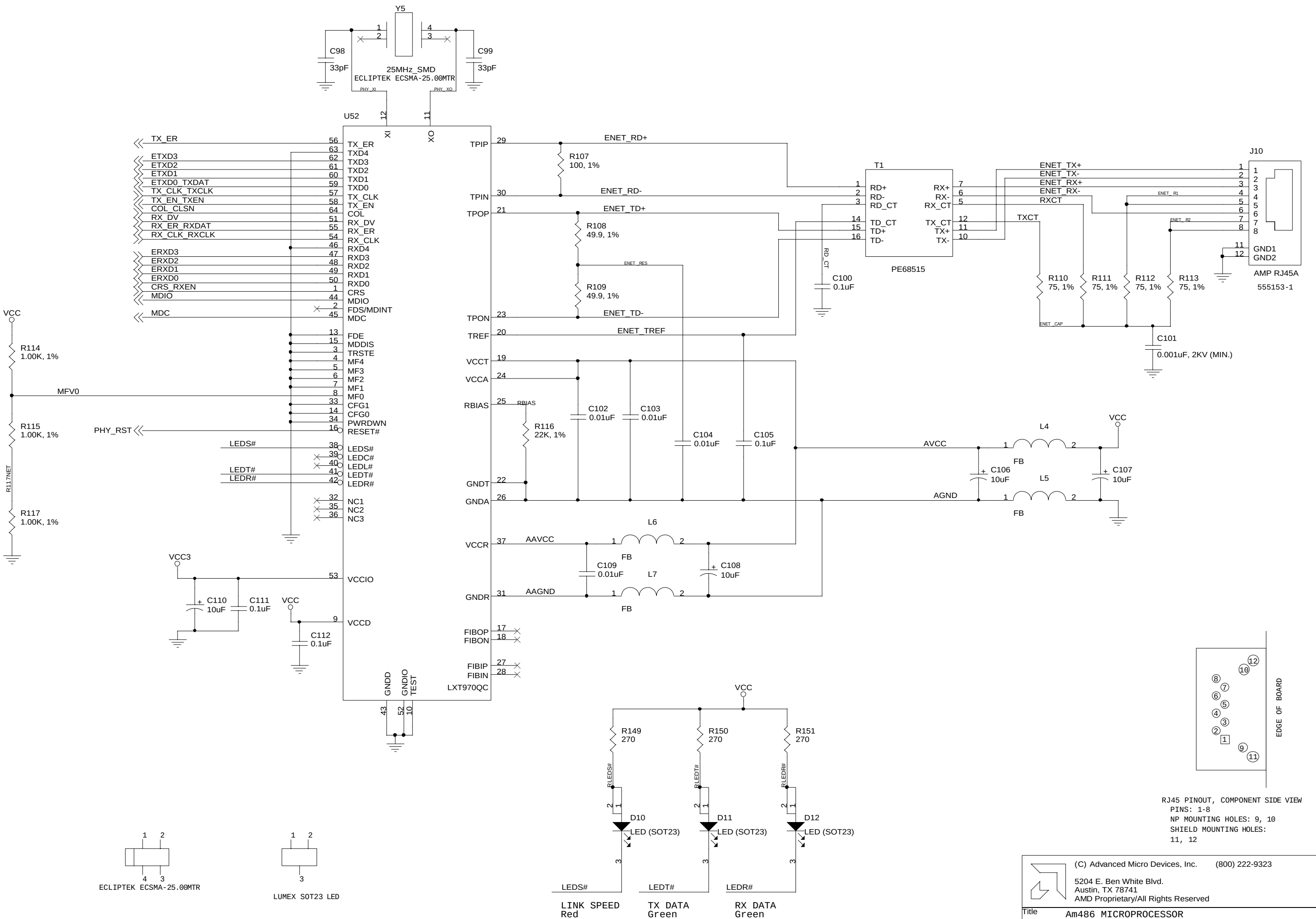
ETHERNET CONTROLLER, BYPASS CAPACITORS AND POWER SUPPLY FOR ETHERNET CONTROLLER, AND SERIAL EEPROMS



(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: ENET1.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 13 of 26

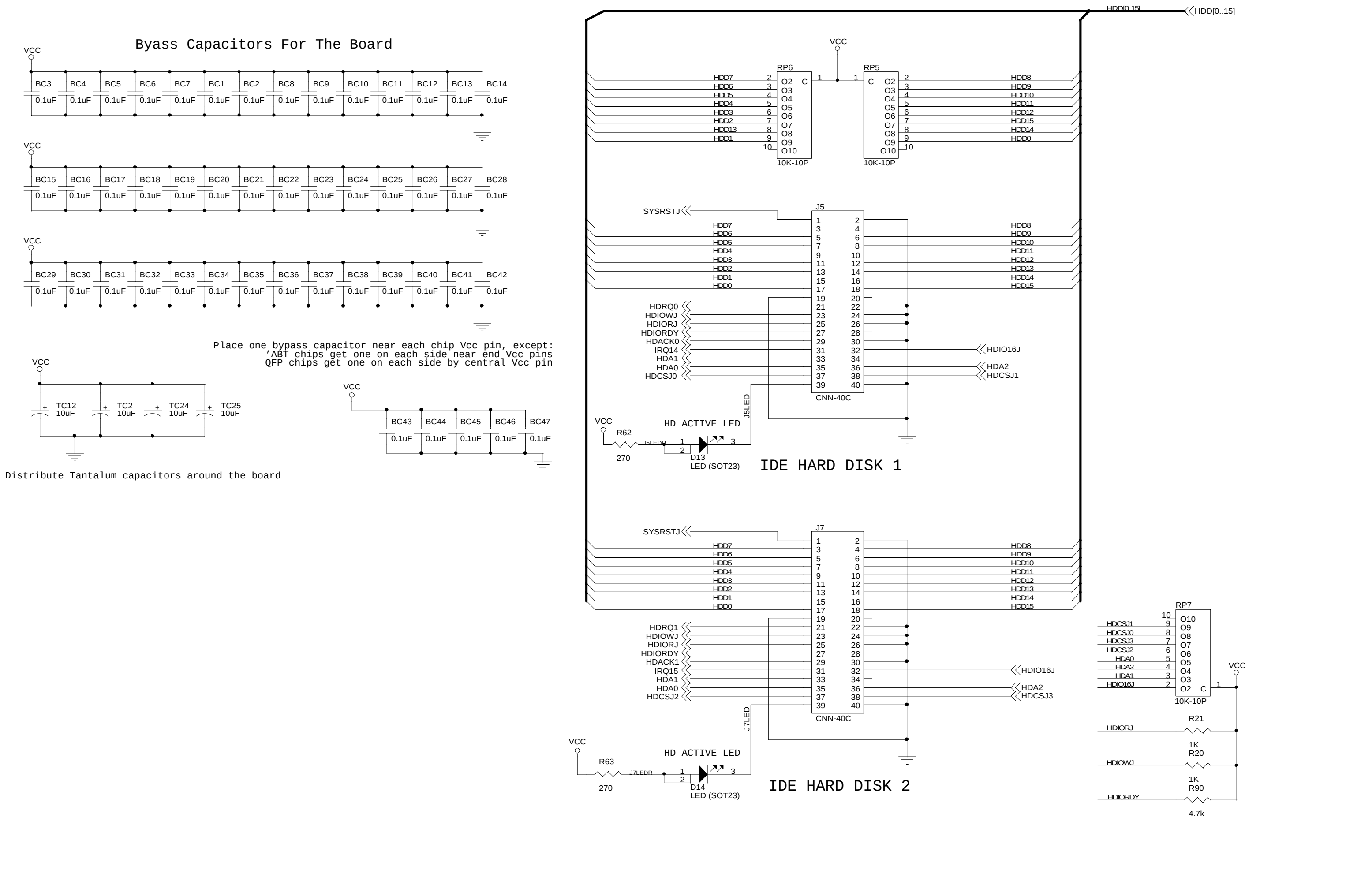
ETHERNET PHY CHIP, ETHERNET CONNECTOR, AND LEDS



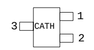
RJ45 PINOUT, COMPONENT SIDE VIEW
PINS: 1-8
NP MOUNTING HOLES: 9, 10
SHIELD MOUNTING HOLES:
11, 12

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number: ENET2.SCH	Rev 2.1
Date: Friday, December 04, 1998	Sheet 14 of 26	

IDE INTERFACE AND BOARD BYPASS CAPACITORS



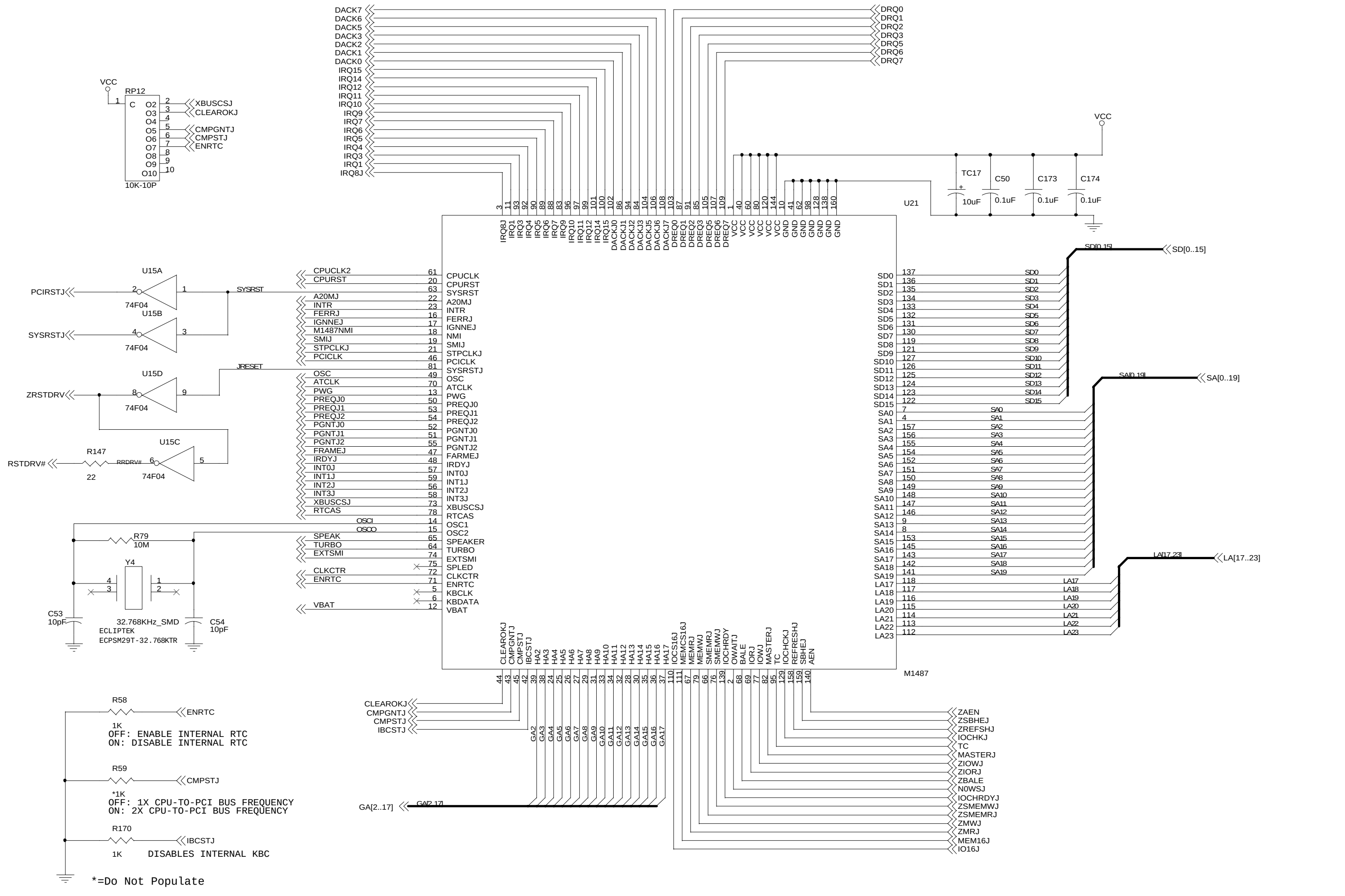
LUMEX LED (SOT23)

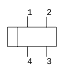


Top View

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: IDE.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	15 of 26

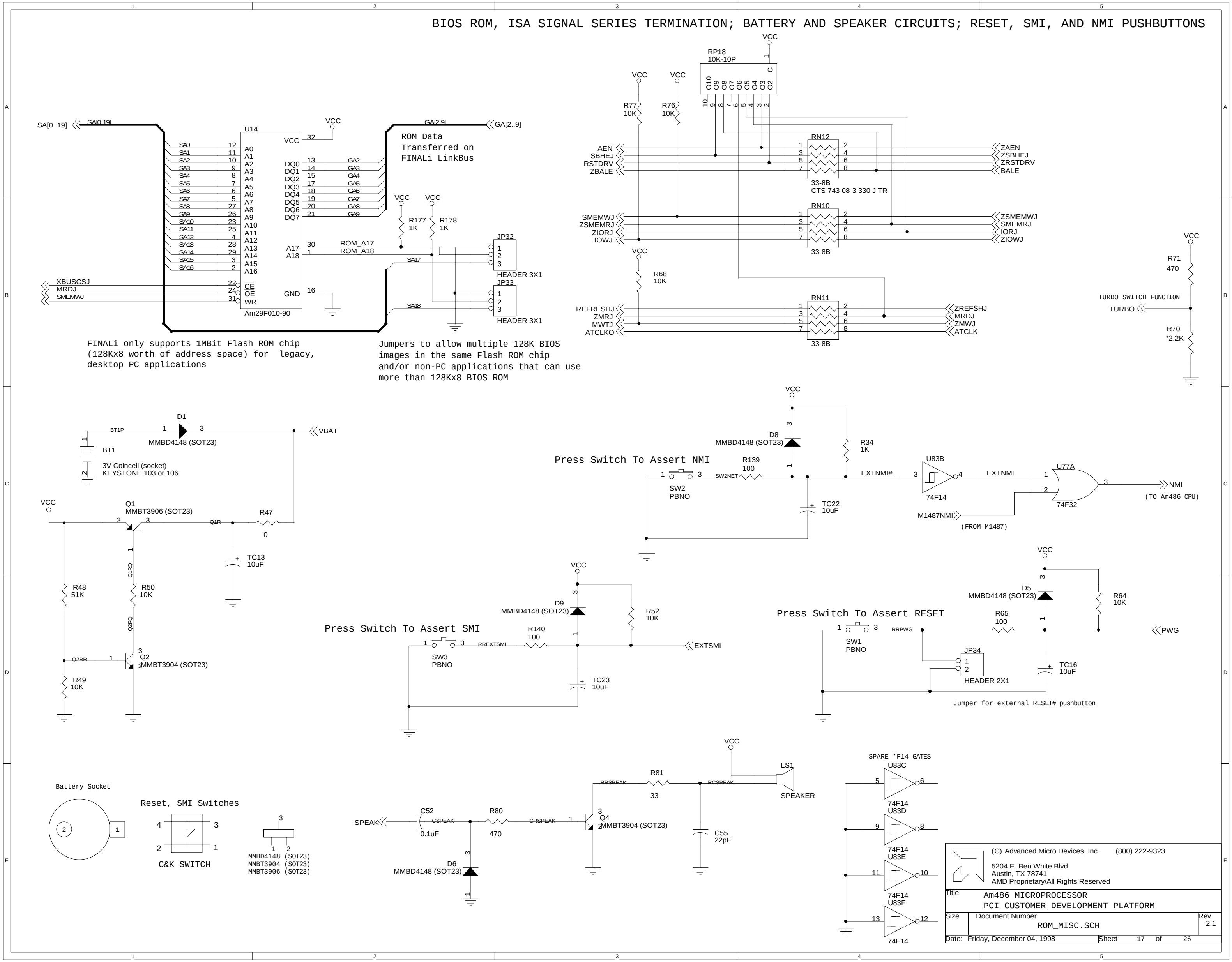
FINALi M1487 INTERFACE



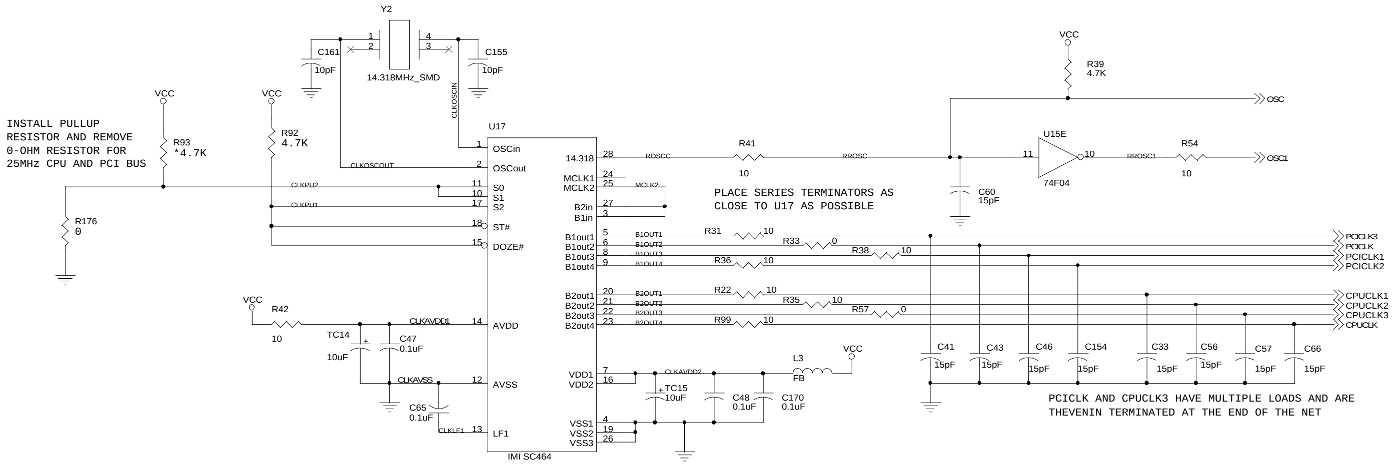


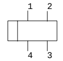
ECLIPTEK ECPSM29T-32.768KTR
(COMPONENT SIDE VIEW)

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	M1487.SCH
Rev	2.1
Date	Friday, December 04, 1998
Sheet	16 of 26


BIOS ROM, ISA SIGNAL SERIES TERMINATION; BATTERY AND SPEAKER CIRCUITS; RESET, SMI, AND NMI PUSHBUTTONS
SA[0..19]
U14
Am29F010-90
GA[2..9]
ROM Data Transferred on FINALi LinkBus
XBUSCSJ
MRDJ
SMEMWJ
ROM_A17
ROM_A18
R177 1K
R178 1K
JP32 HEADER 3X1
JP33 HEADER 3X1
FINALi only supports 1MBit Flash ROM chip (128Kx8 worth of address space) for legacy, desktop PC applications
Jumpers to allow multiple 128K BIOS images in the same Flash ROM chip and/or non-PC applications that can use more than 128Kx8 BIOS ROM
RP18 10K-10P
R77 10K
R76 10K
AEN
SBHEJ
RSTDRV
ZBALE
RN12 33-8B
CTS 743 08-3 330 J TR
ZAEN
ZSBHEJ
ZRSTDRV
BALE
SMEMWJ
ZSMEMRJ
ZIORJ
IOWJ
RN10 33-8B
ZSMEMWJ
SMEMRJ
IORJ
ZIOWJ
R68 10K
REFRESHJ
ZMRJ
MWTJ
ATCLKO
RN11 33-8B
ZREFSHJ
MRDJ
ZMWJ
ATCLK
R71 470
TURBO SWITCH FUNCTION
TURBO
R70 *2.2K
D1 MMBD4148 (SOT23)
VBAT
BT1
3V Coincell (socket)
KEYSTONE 103 or 106
Q1 MMBT3906 (SOT23)
R47 0
TC13 10uF
R48 51K
R50 10K
Q2 MMBT3904 (SOT23)
R49 10K
D8 MMBD4148 (SOT23)
R34 1K
Press Switch To Assert NMI
SW2 PBNO
R139 100
TC22 10uF
U83B 74F14
EXTNMI#
EXTNMI
U77A 74F32
NMI
(TO Am486 CPU)
M1487NMI
(FROM M1487)
D9 MMBD4148 (SOT23)
R52 10K
Press Switch To Assert SMI
SW3 PBNO
R140 100
TC23 10uF
EXTSMI
D5 MMBD4148 (SOT23)
R64 10K
Press Switch To Assert RESET
SW1 PBNO
R65 100
PWG
JP34 HEADER 2X1
TC16 10uF
Jumper for external RESET# pushbutton
LS1 SPEAKER
R81 33
C55 22pF
Q4 MMBT3904 (SOT23)
SPEAK
C52 0.1uF
R80 470
D6 MMBD4148 (SOT23)
SPARE 'F14 GATES
U83C 74F14
U83D 74F14
U83E 74F14
U83F 74F14
Battery Socket
Reset, SMI Switches
C&K SWITCH
MMBD4148 (SOT23)
MMBT3904 (SOT23)
MMBT3906 (SOT23)
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved
Title Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM
Size Document Number ROM_MISC.SCH Rev 2.1
Date: Friday, December 04, 1998 Sheet 17 of 26

CLOCK GENERATOR





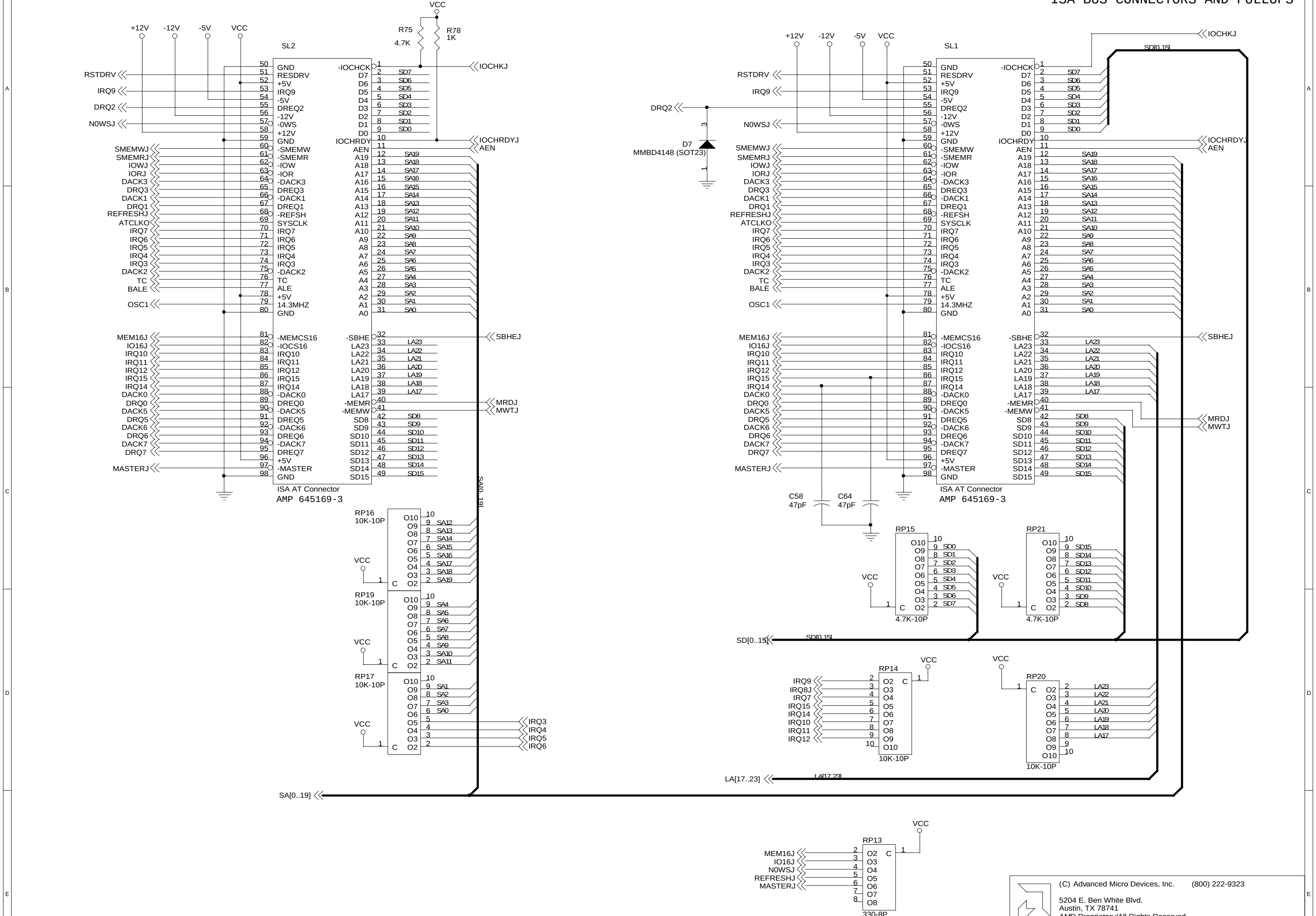
ECLIPTEK ECSMAT-14.318MTR
(COMPONENT SIDE VIEW)

Title: Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM

Size | Document Number: CLOCK.SCH | Rev 2.1

Date: Friday, December 04, 1998 | Sheet 18 of 26

ISA BUS CONNECTORS AND PULLUPS



(C) Advanced Micro Devices, Inc. (800) 222-9323

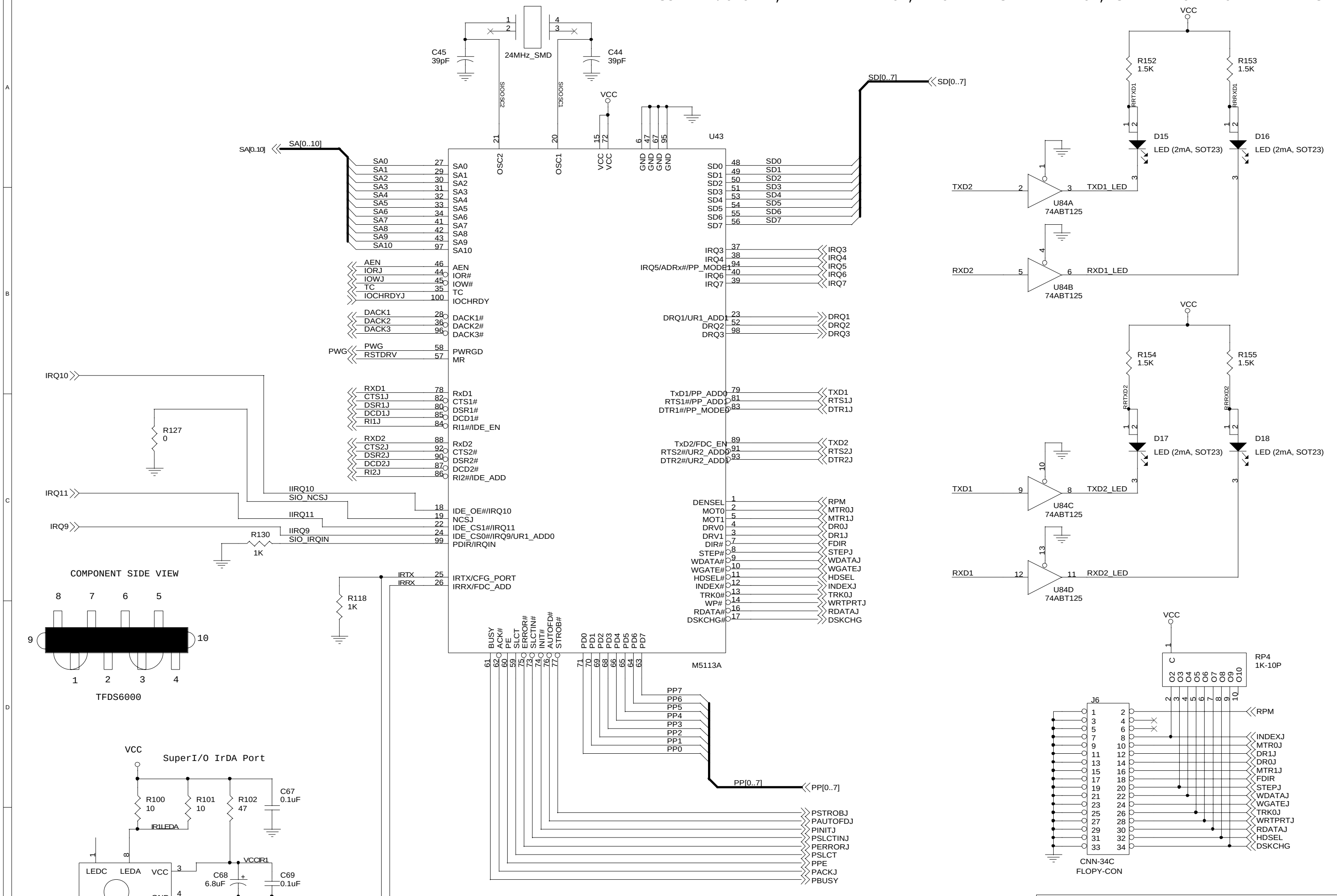
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved

Title: Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM

Size | Document Number: ISA_CONN.SCH | Rev 2.1

Date: Friday, December 04, 1998 | Sheet 19 of 26

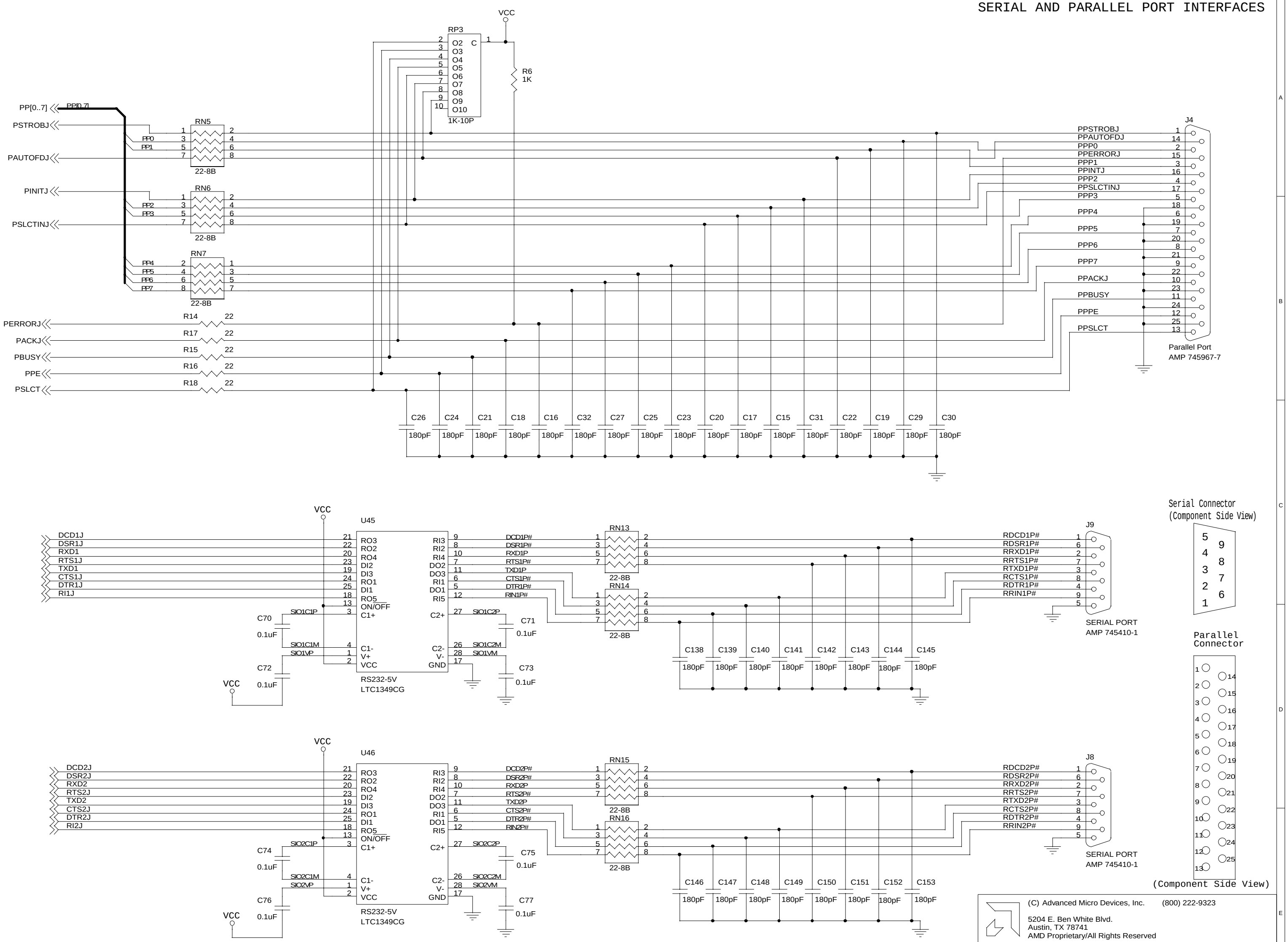
SUPER I/O CHIP, IrDA INTERFACE, FLOPPY DISK INTERFACE, SERIAL PORT ACTIVITY LEDS



(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741

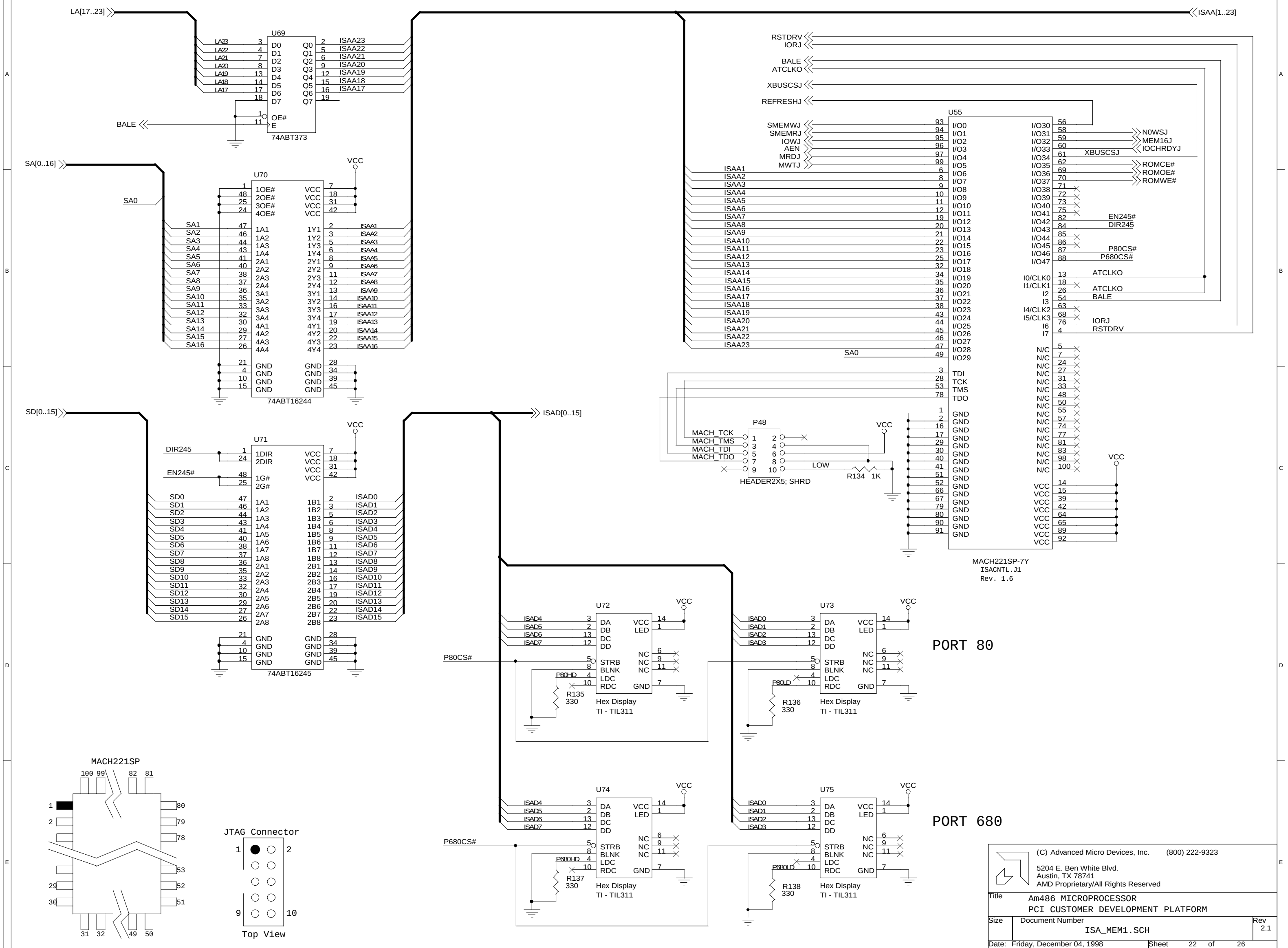
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	SUPER_I/O.SCH
Rev	2.1
Date	Friday, December 04, 1998
Sheet	20 of 26

SERIAL AND PARALLEL PORT INTERFACES



Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	SERIAL_PARALLEL.SCH
Rev	2.1
Date	Friday, December 04, 1998
Sheet	21 of 26

INTERFACE FOR ISA BUS MEMORY AND HEX DISPLAYS

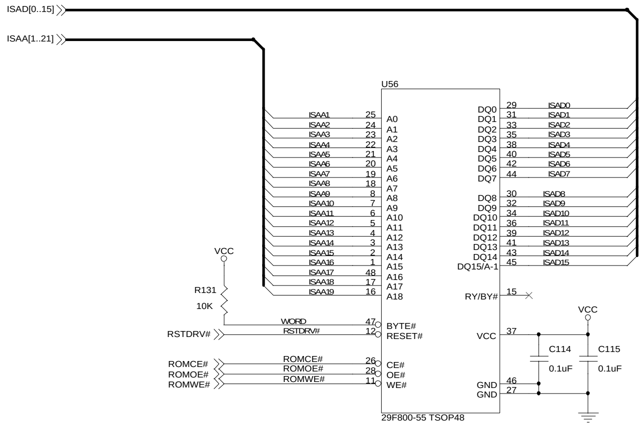


(C) Advanced Micro Devices, Inc. (800) 222-9323

5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size / Document Number	ISA_MEM1.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	22 of 26

ISA BUS FLASH MEMORY



1MByte ISA Flash Memory

Configured as 512Kx16bit (29F800T device in "word" mode)

Access at even ISA Memory addresses between 15MB and 16MB-1

Use CSR 12h bit 3 to access 0f00000-0ffffffh as ISA Memory (instead of DRAM, if installed)

Flash chip A0 pin tied to ISA Address Bit 1; mulitply desired
Flash chip address by 2h to find correct ISA address for access
(ex: Flash chip address 555h is accessed at ISA address AAAh)

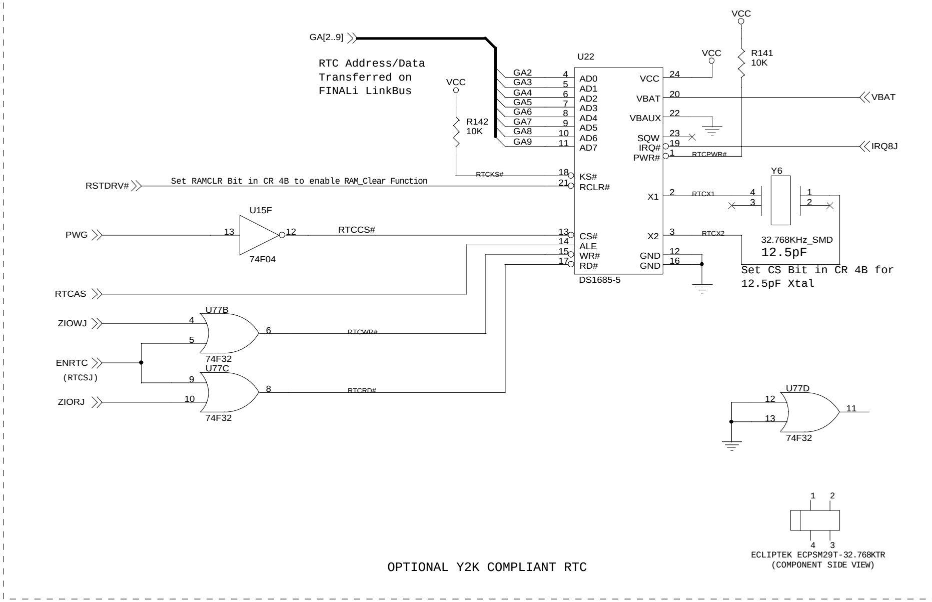
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741

Title: Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM

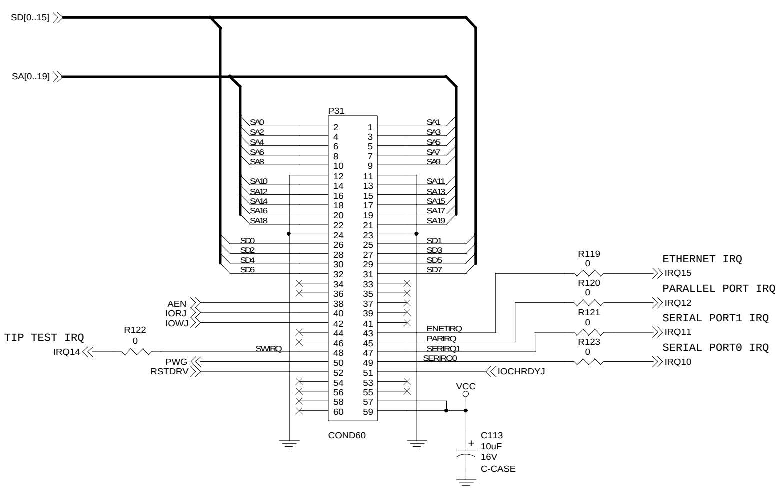
Size | Document Number: ISA_MEM2.SCH | Rev 2.1

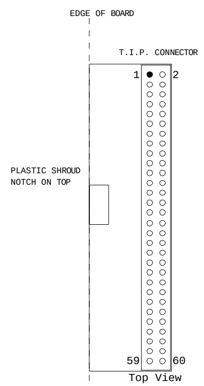
Date: Friday, December 04, 1998 | Sheet 23 of 26

OPTIONAL Y2K RTC AND TEST INTERFACE PORT CONNECTOR



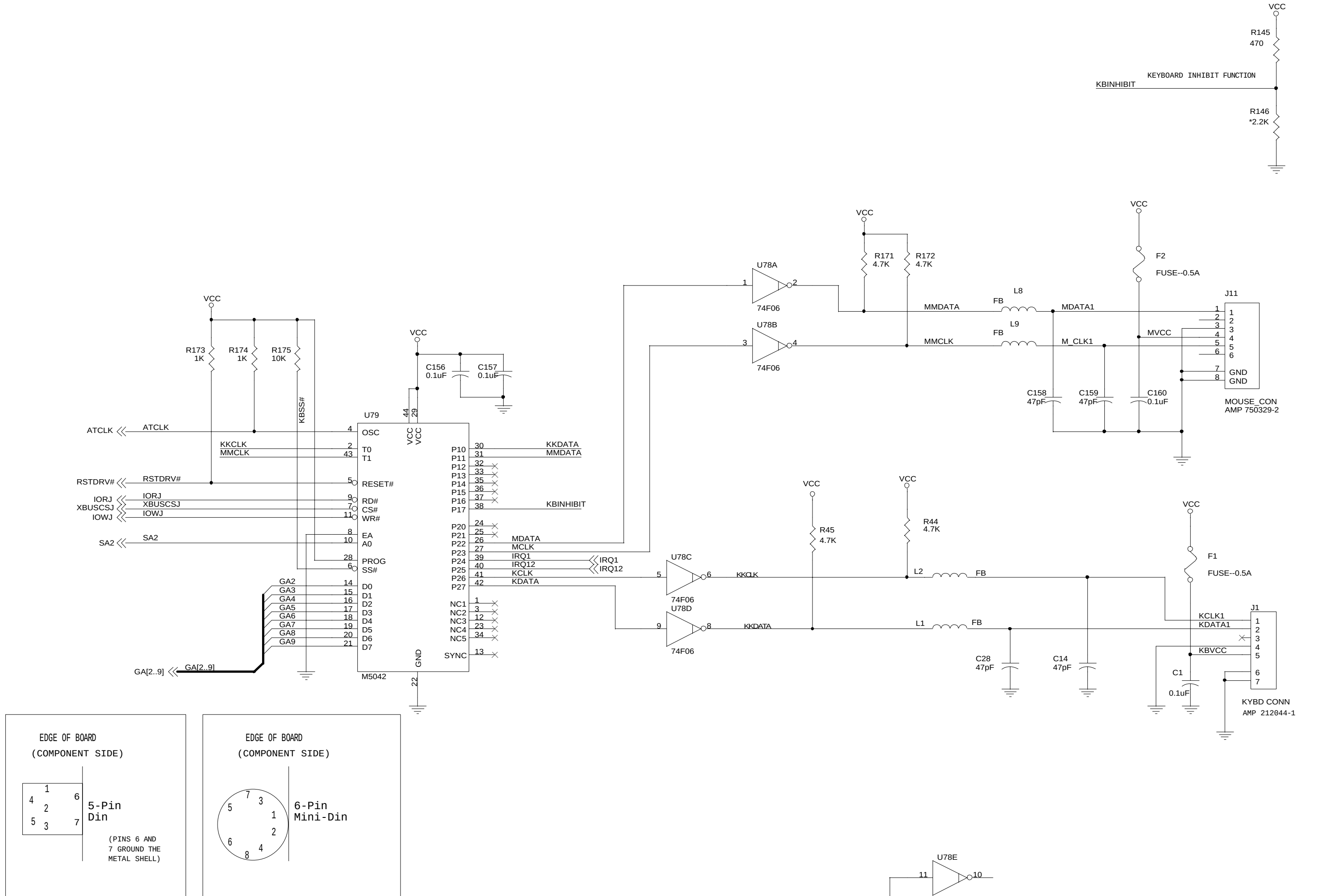
T.I.P.
CONNECTOR





Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number RTC_TIP.SCH	Rev 2.1
Date: Friday, December 04, 1998	Sheet 24 of 26	

PC KEYBOARD AND MOUSE INTERFACE



(C) Advanced Micro Devices, Inc. (800) 222-9323

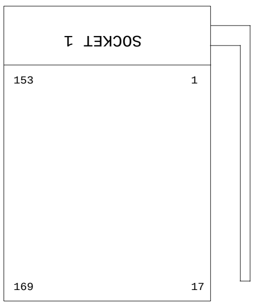
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: KEYBOARD.SCH
Rev	2.1
Date:	Friday, December 04, 1998
Sheet	25 of 26

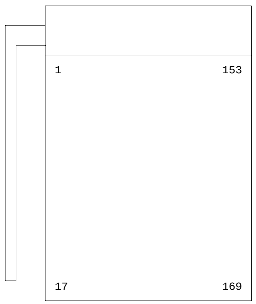
SOCKET1
Am486 MICROPROCESSOR
(PIN #)-PIN DESIGNATION
(PIN SIDE VIEW)

(1)-D20	(18)-D19	(35)-D11	(52)-D9	(59)-GND	(65)-DP1	(71)-GND	(77)-GND	(83)-INC	(89)-GND	(95)-GND	(101)-GND	(107)-D2	(113)-D0	(119)-A31	(136)-A28	(153)-A27
(2)-D22	(19)-D21	(36)-D18	(53)-D13	(60)-VCC	(66)-D8	(72)-VCC	(78)-D3	(84)-D5	(90)-VCC	(96)-D6	(102)-VCC	(108)-D1	(114)-A29	(120)-GND	(137)-A25	(154)-A26
(3)-TCK	(20)-GND	(37)-CLK	(54)-D17	(61)-D10	(67)-D15	(73)-D12	(79)-DP2	(85)-D16	(91)-D14	(97)-D7	(103)-D4	(109)-DP0	(115)-A30	(121)-A17	(138)-VCC	(155)-A23
(4)-D23	(21)-GND	(38)-VCC	(55)-SKT1_NC											(122)-A19	(139)-GND	(156)-VOLDET
(5)-DP3	(22)-GND	(39)-VCC												(123)-A21	(140)-A18	(157)-A14
(6)-D24	(23)-D25	(40)-D27												(124)-A24	(141)-VCC	(158)-GND
(7)-GND	(24)-VCC	(41)-D26												(125)-A22	(142)-A15	(159)-A12
(8)-D29	(25)-D31	(42)-D28												(126)-A20	(143)-VCC	(160)-GND
(9)-GND	(26)-VCC	(43)-D30												(127)-A16	(144)-VCC	(161)-GND
(10)-INV	(27)-SMI#	(44)-SRESET												(128)-A13	(145)-VCC	(162)-GND
(11)-GND	(28)-VCC	(45)-UP#												(129)-A9	(146)-VCC	(163)-GND
(12)-HITM#	(29)-CACHE#	(46)-SMIACT#												(130)-A5	(147)-A11	(164)-GND
(13)-INC	(30)-WB/WT#	(47)-INC												(131)-A7	(148)-A8	(165)-A10
(14)-TDI	(31)-TMS	(48)-FERR#												(132)-A2	(149)-VCC	(166)-GND
(15)-IGNEE#	(32)-NMI	(49)-FLUSH#	(56)-A20M#	(62)-HOLD	(68)-KEN#	(74)-STPCLK#	(80)-BRDY#	(86)-BE2#	(92)-BE0#	(98)-PWT	(104)-D/C#	(110)-LOCK#	(116)-HLDA	(133)-BREQ	(150)-A3	(167)-A6
(16)-INTR	(33)-TDO	(50)-RESET	(57)-BS8#	(63)-VCC	(69)-RDY#	(75)-VCC	(81)-VCC	(87)-BE1#	(93)-VCC	(99)-VCC	(105)-VCC	(111)-M/IO#	(117)-VCC	(134)-PLOCK#	(151)-BLAST#	(168)-A4
(17)-AHOLD	(34)-EADS#	(51)-BS16#	(58)-BOFF#	(64)-GND	(70)-BE3#	(76)-GND	(82)-GND	(88)-PCD	(94)-GND	(100)-GND	(106)-GND	(112)-W/R#	(118)-GND	(135)-PCHK#	(152)-CLKMUL	(169)-ADS#

Am486 MICROPROCESSOR
PIN SIDE VIEW



COMPONENT SIDE VIEW



SOLDER SIDE VIEW

Title: Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM

Size | Document Number: CPU_PINOUT.SCH | Rev 2.1

Date: Friday, December 04, 1998 | Sheet 26 of 26

Index

Numerics

A

B

C

D

E

F

G

H

I

J

K

L

M

T

U

V

W

Y

Z